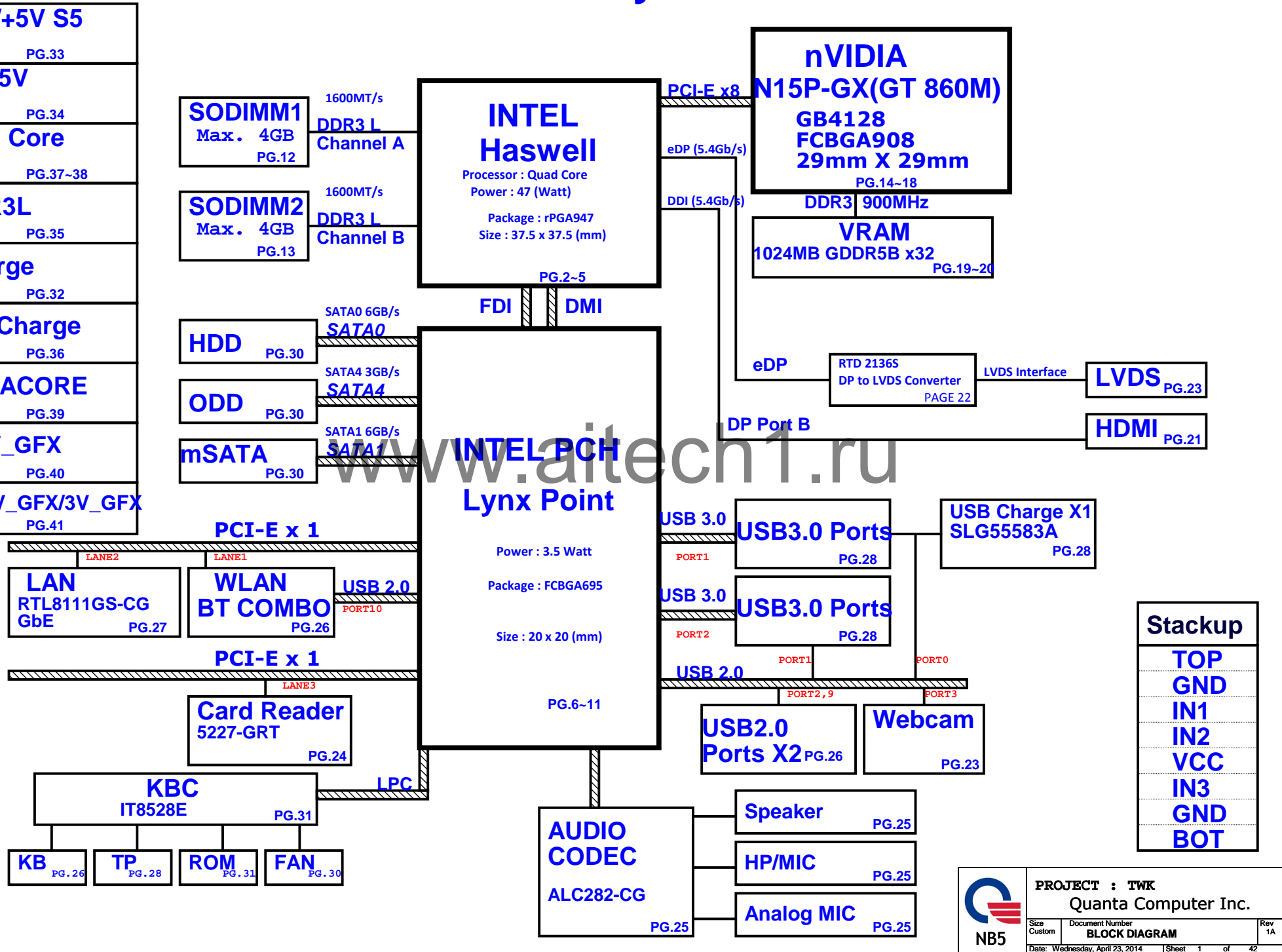
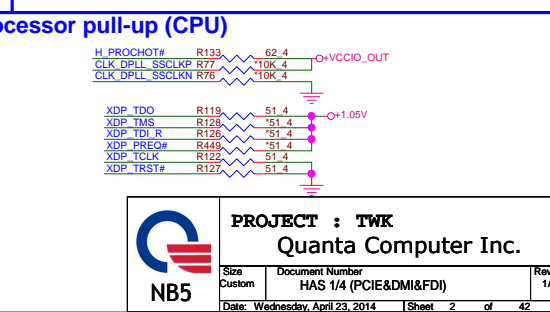
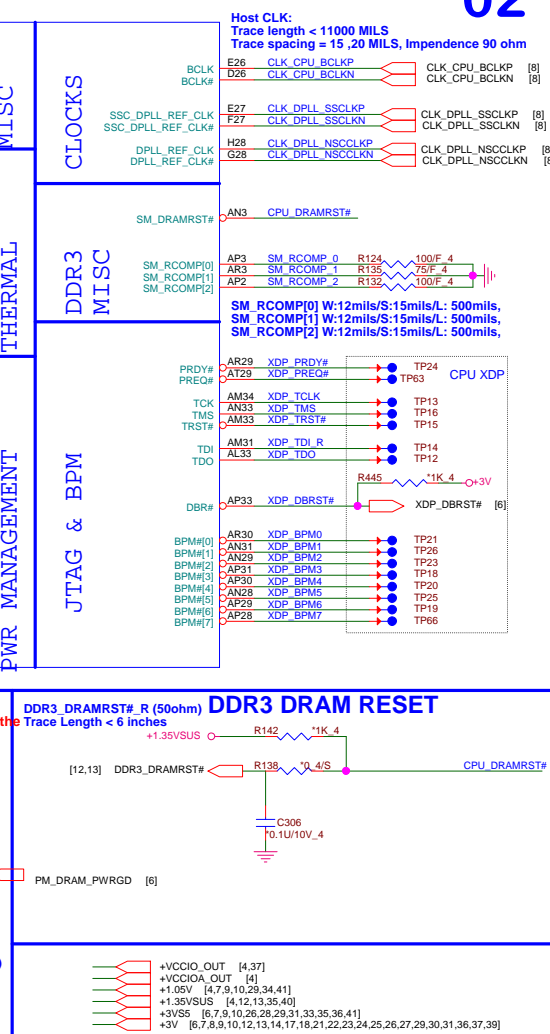


# TWK Shark Bay DIAGRAM

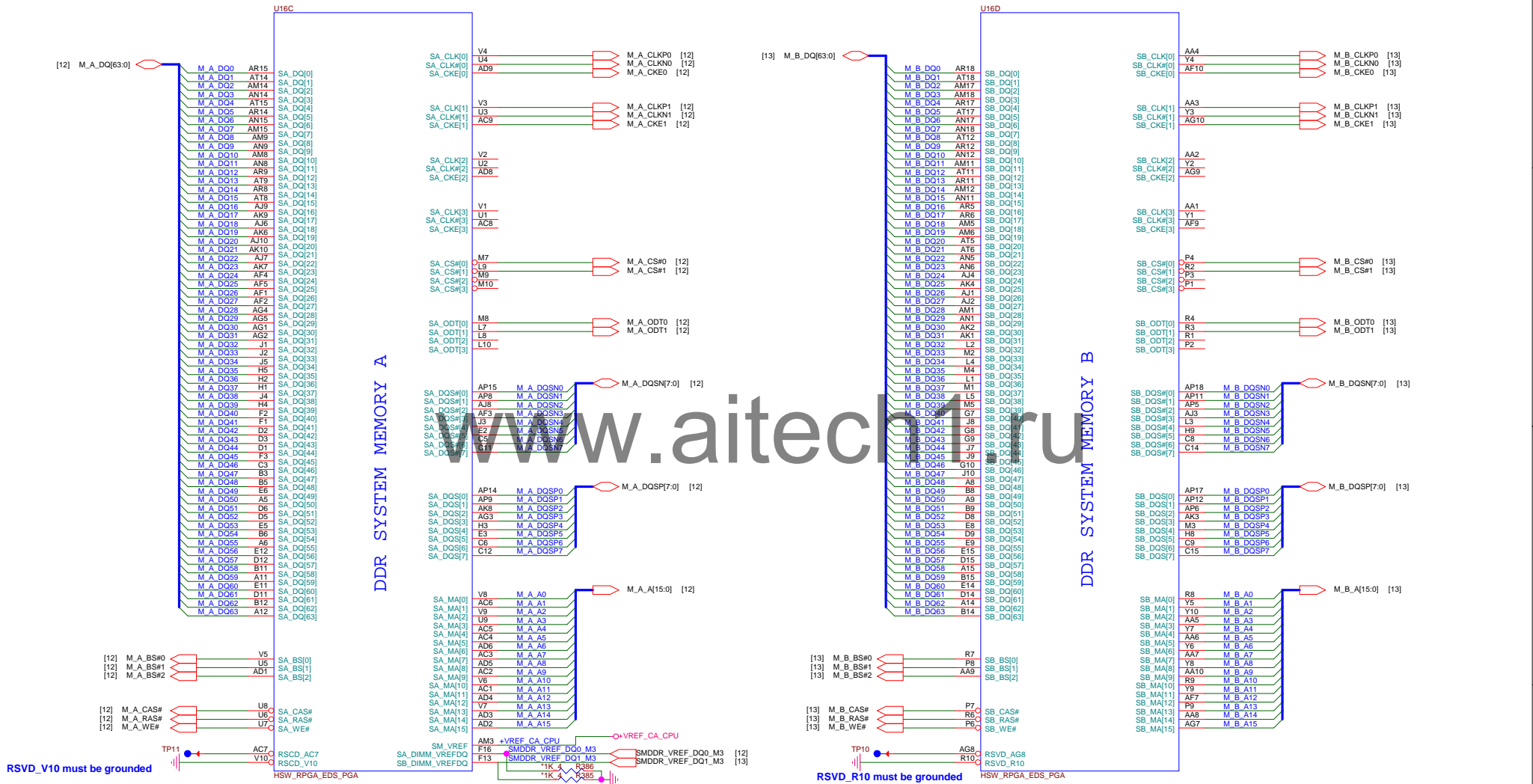
01






# Haswell Processor (DDR3)

03



CPU SM\_VREF

		<b>PROJECT : TWK</b> <b>Quanta Computer Inc.</b>	
Size	Document Number	Rev	
Custom	HAS 2/4 (DDR3 I/F)	1A	
Date: Wednesday, April 23, 2014		Sheet	3 of 42

## Haswell Processor (POWER)

+VCCIN 95A

## POWER

U16F

+VCC\_CORE

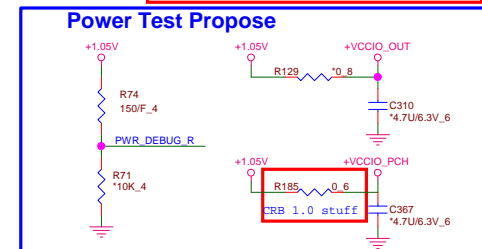
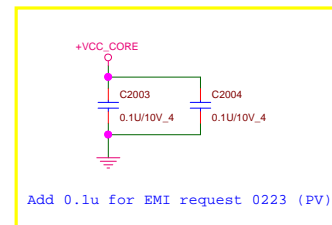
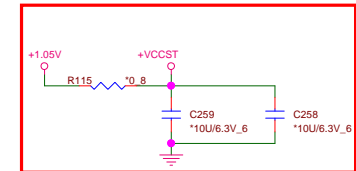
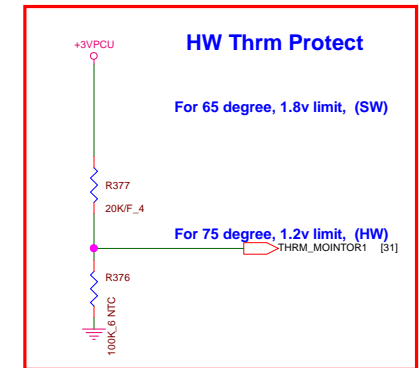
+1.35VSUS 4.2A

+1.35VSUS

## VDDQ Output Decoupling Recommendations

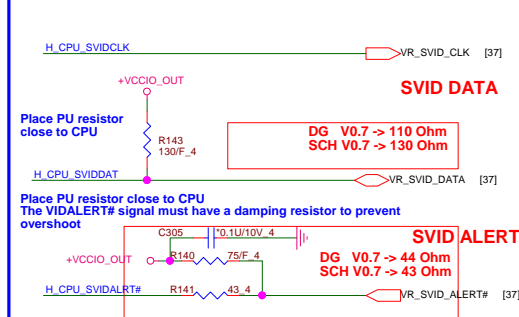
330uFx2	7343	BOT socket side
22uFx11	0805	5 on TOP, 6 on BOT inside socket cavity
10uFx10	0805	5 on TOP, 5 on BOT inside socket cavity

+VCCIOA_OUT	[2]
+VCCIO_OUT	[2,37]
+VCCIO_PCH	[10]
+1.5V	[6,7,8,10,25,26,29,30,35]
+1.05V	[2,7,9,10,23,34,41]
+VCC_CORE	[37,38]
+VCCST	[2]
+1.35VSUS	[2,12,13,35,40]



## CPU VDDQ

Layout note: It is recommended to shield VIDSOUT signal by routing it in between the VIDSKL and VIDALERT# signals.



**VCC Output Decoupling Recommendations**

470uFx4	7343	TOP socket side
22uFx8	0805	4 on TOP, 4 on BOT near socket edge
22uFx11	0805	TOP, inside socket cavity
10uFx11	0805	BOT, inside socket cavity

## CORE SUPPLY

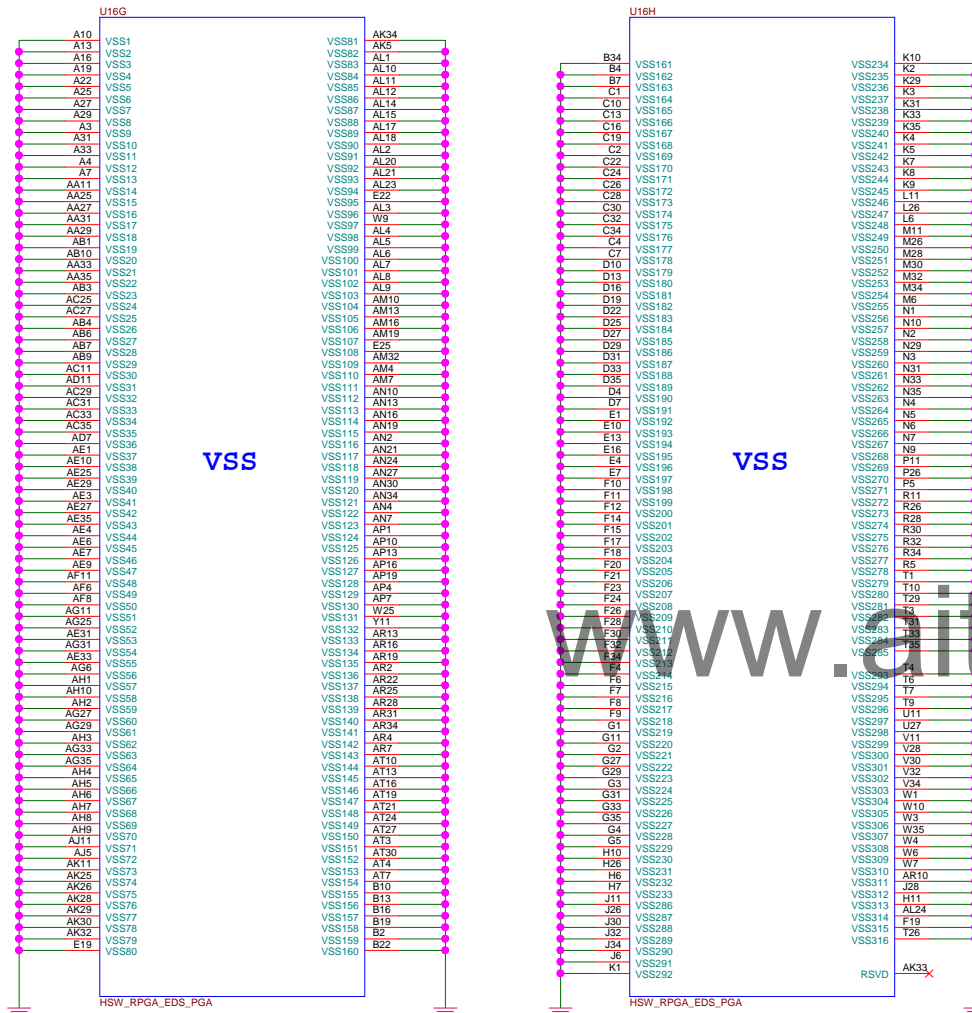
## SVID

## SENSE LINES

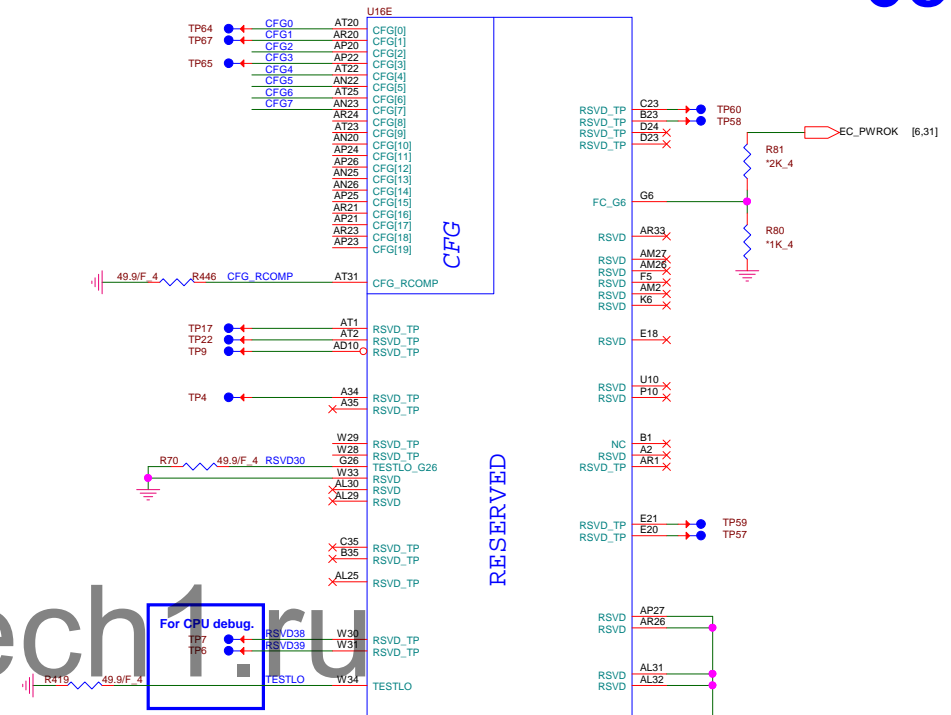
www.aitech1.ru



## Haswell Processor (GND)



## Haswell Processor (RESERVED, CFG)



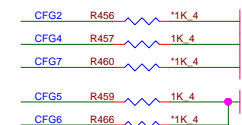
CFG[3] (PHYSICAL_DEBUG_ENABLED (DFX PRIVACY))
0 Enable; SET DFX ENABLED BIT IN DEBUG

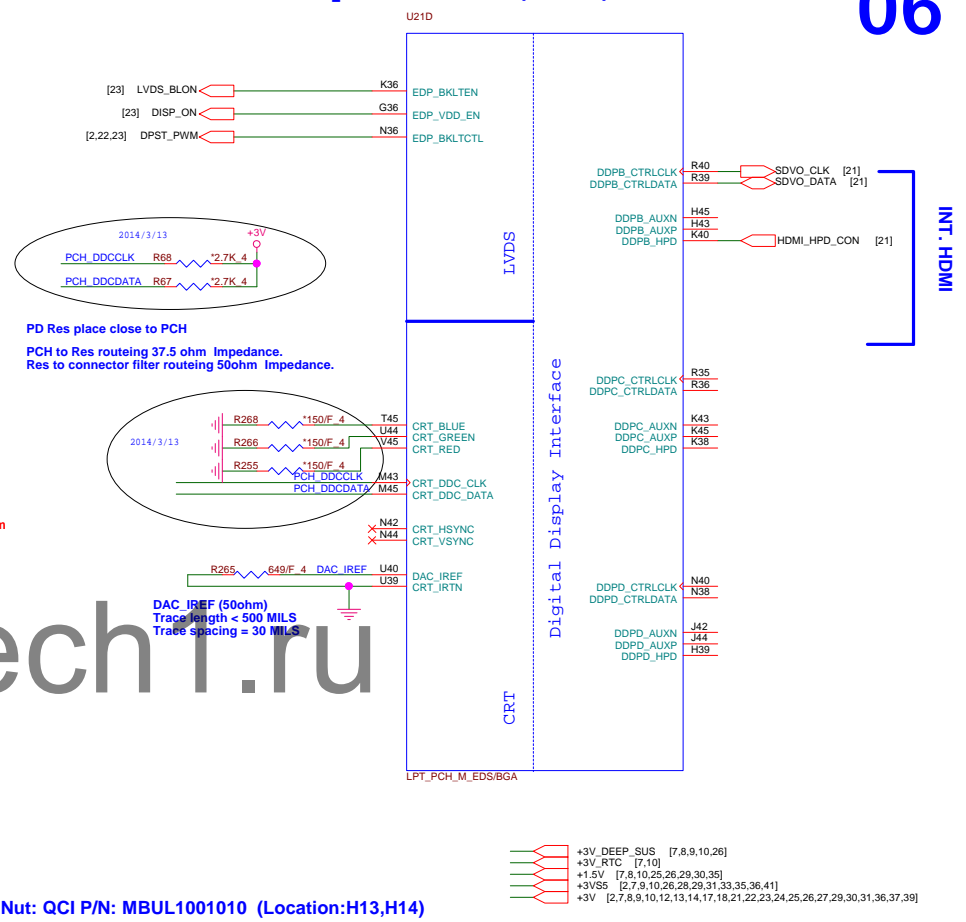
```
CFG[6:5] (PCIe Port Bifurcation Straps)
11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
```

## Processor Strapping

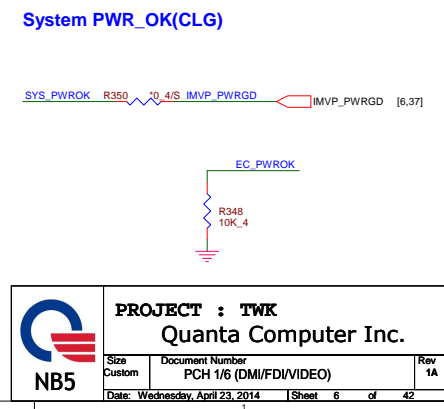
The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training





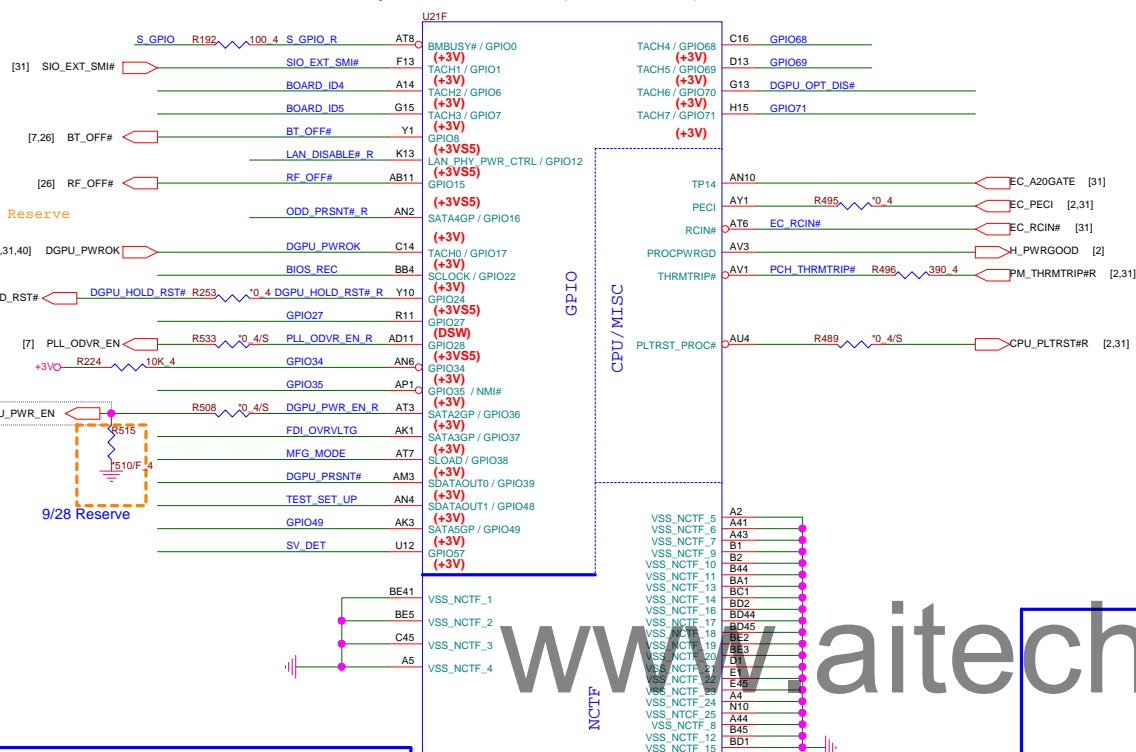
**PCH Nut: QCI P/N: MBUL1001010 (Location:H13,H14)**





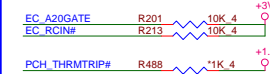


## Lynx Point (GPIO,VSS\_NCTF,RSVD)

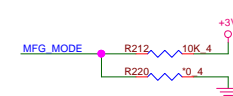


+3V\_DEEP\_SUS [6,7,8,10,26]  
+3V55 [2,6,7,10,26,28,29,31,33,35,36,41]  
+3V [2,6,7,8,10,12,13,14,17,18,21,22,23,24,25,26,27,29,30,31,36,37,39]  
+5V55 [25,29,33,34,35,36,37,38,39,40]

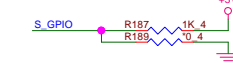
## PCH MISC PU/PD



## MFG-TEST



## Swap GPIO

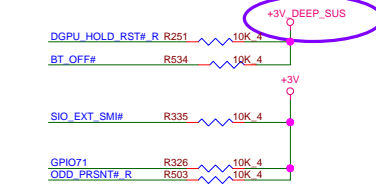


0 = SGPIO  
1 = Default

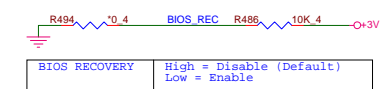
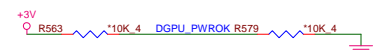
Intel ME Crypto Transport Layer Security (TLS) cipher suite

Low = Disable (Default)  
High = Enable

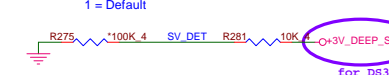
## GPIO Pull-up/Pull-down(CLG)



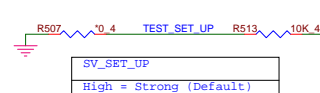
DGPU\_PWROK UMA=0



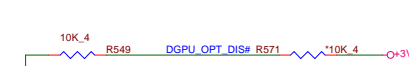
## SV Detect



## BIOS\_RESP



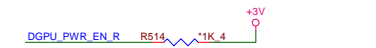
## DGPU\_OPT\_DIS# GPIO70 Optimus=0, Dis only=1



## SATA3GP/GPIO37 TLS Confidentiality

0 = TLS no confidentiality (Int PD)  
1 = TLS with confidentiality

## GPIO36 Internal PD



## GFX Present GPIO39 Optimus=1, UMA=0



SG	UMA
Stuff	Ra
NC	Rb



PROJECT : TWK  
Quanta Computer Inc.

Size Custom Document Number PCH 4/6 (GPIO/MISC) Rev 1A  
Date: Wednesday, April 23, 2014 Sheet 9 of 42

## HSW BOARD ID SETTING

BOARD_ID0	GPIO44	MODEL BIT0
BOARD_ID1	GPIO45	MODEL BIT1
BOARD_ID2	GPIO46	MODEL BIT2
BOARD_ID3	GPIO4	MODEL BIT3
BOARD_ID4	GPIO6	MODEL BIT4
BOARD_ID5	GPIO7	No Dolby=0, Dolby=1
GPIO71	GPIO71	Reserve
GPIO35	GPIO35	Reserve
GPIO49	GPIO49	Reserve
GPIO68	GPIO68	Reserve
GPIO69	GPIO69	Reserve
DGPU_PRNT	GPIO39	Optimus=1, UMA=0
DGPU_OPT_DIS#	GPIO70	Optimus=0, Dis only=1

## BOARD\_ID[4:0] Model Name

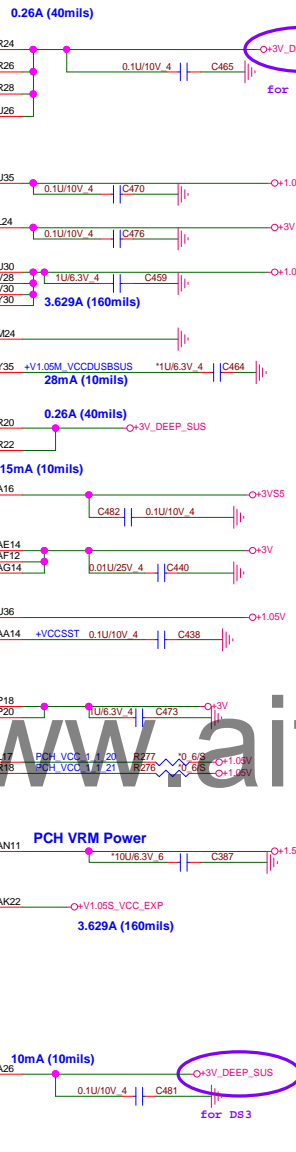
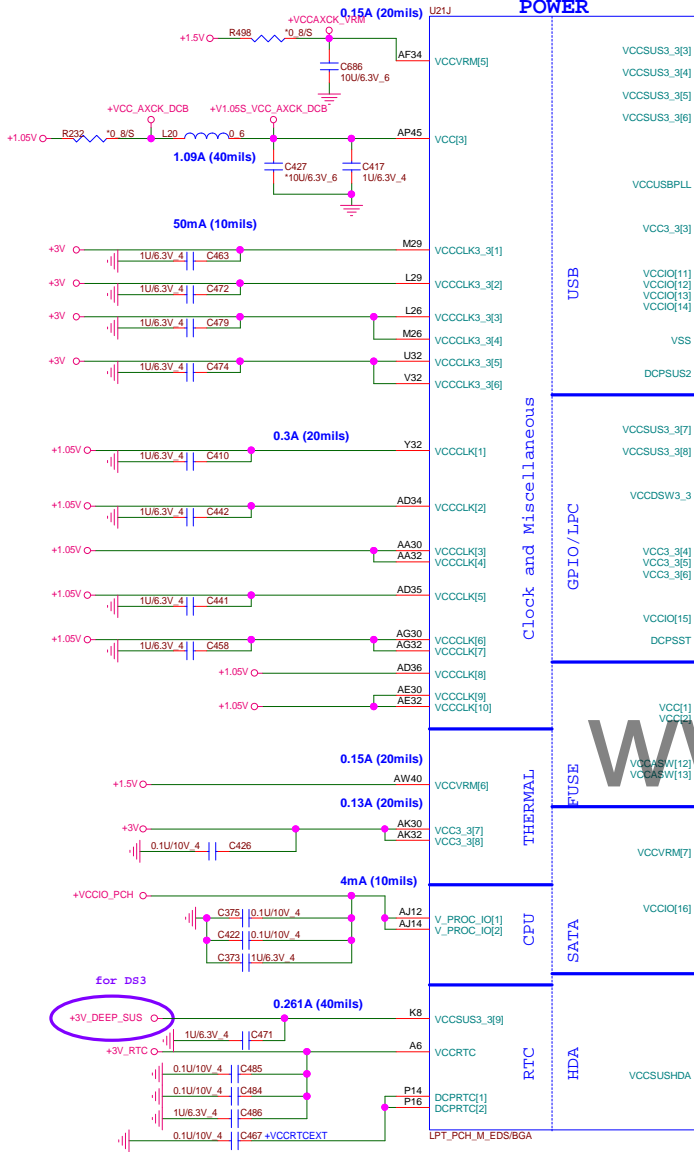
00000	QLGS
00001	TWS
00010	TWJ
00011	TWK

GPIO68	Hi	Lo
	LVDS interface	eDP interface

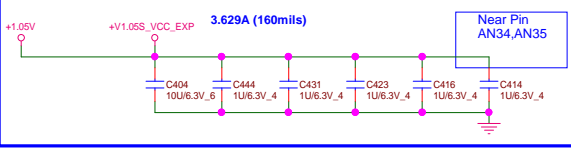


# Lynx Point (POWER)

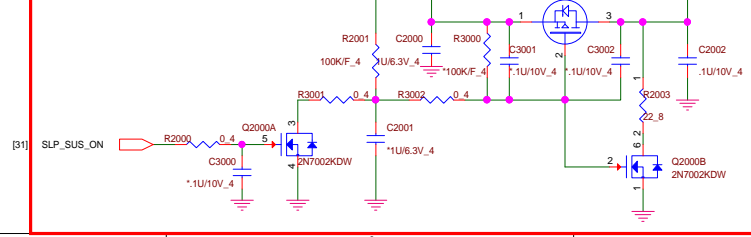
## POWER



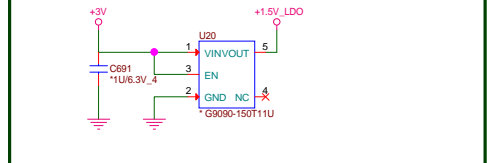
### PCH VCCIO Power



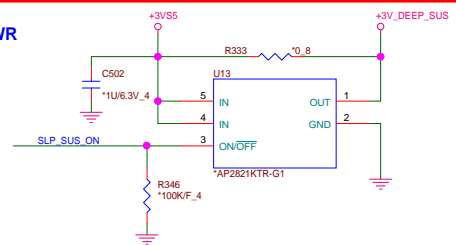
Add sch for DS3 PWR (PV) 02/19  
Modify DS3 (PQ) 4/10



If have power noise issue then stuff it.

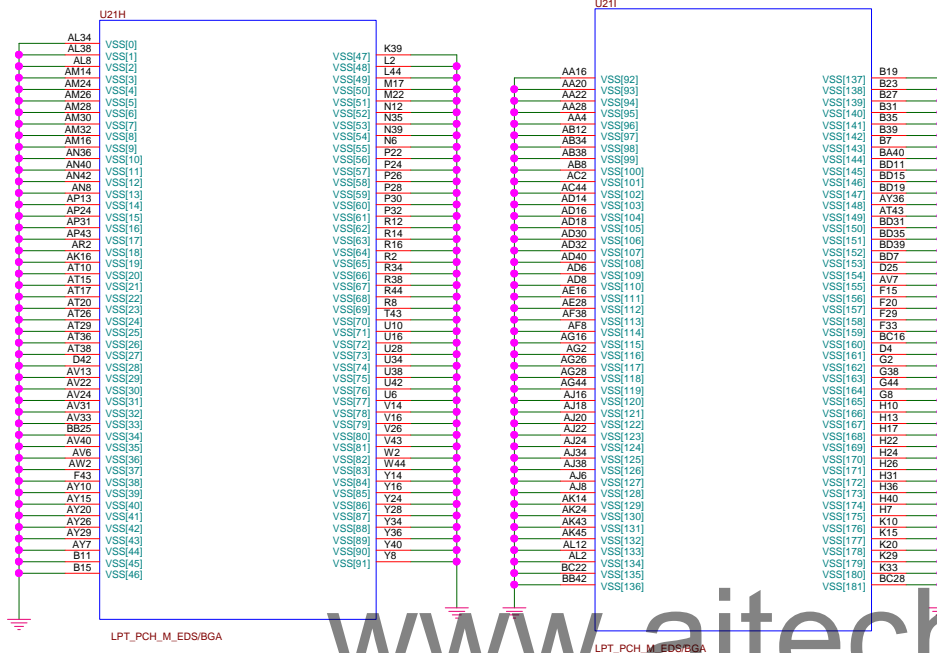


### PCH DS3 PWR

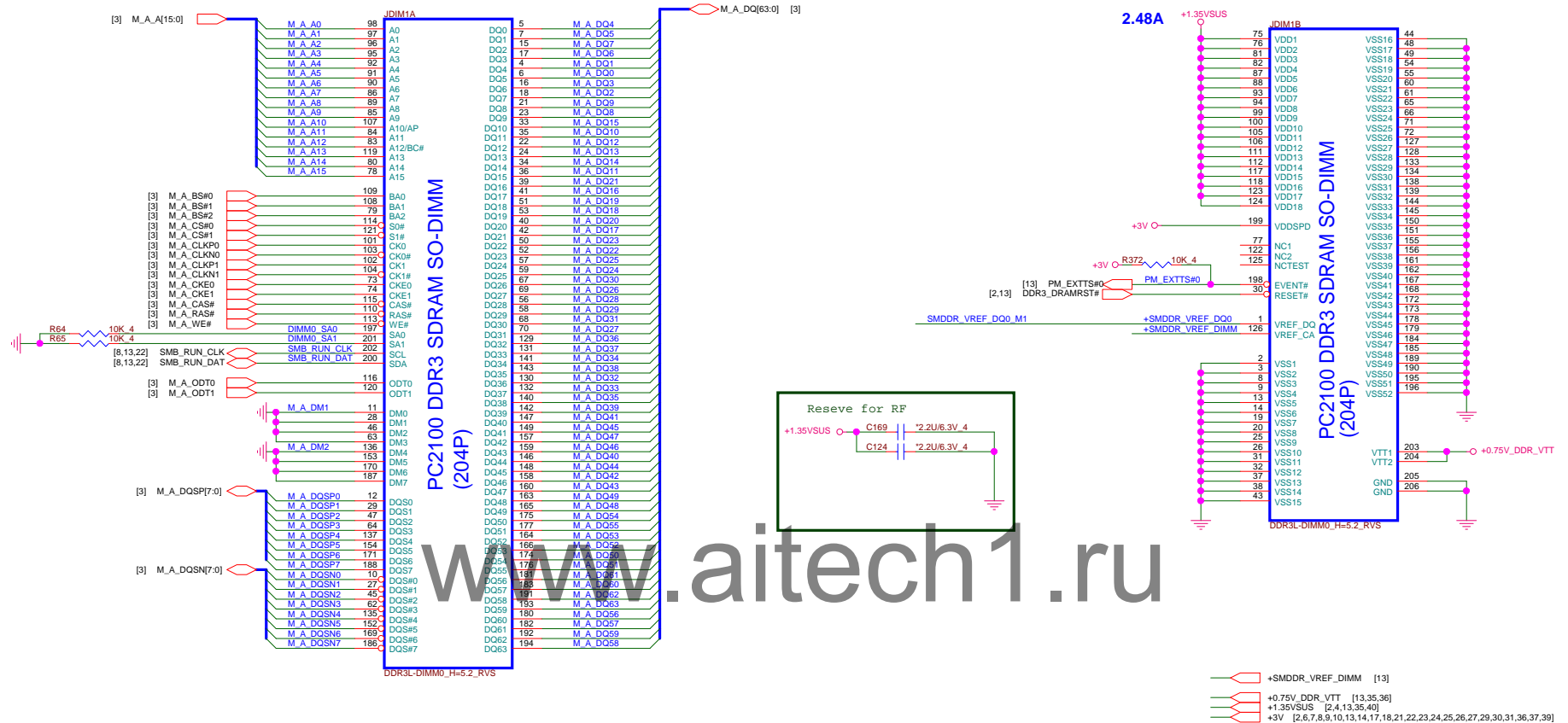




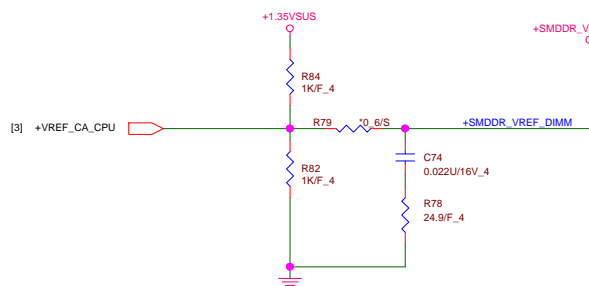
# Lynx Point (GND)



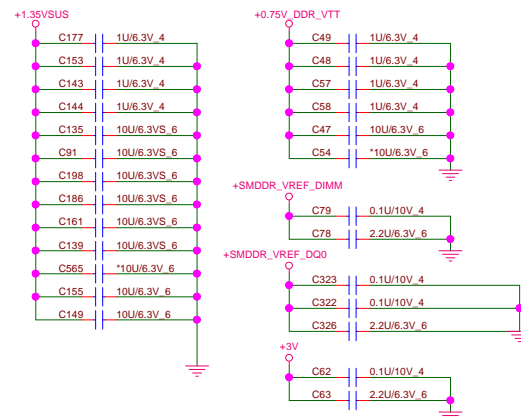
www.aitech1.ru



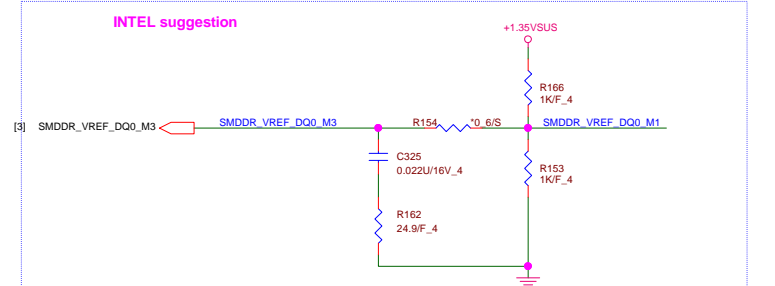
## 10/4 : INTEL suggestion



## Place these Caps near So-Dimm0.

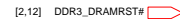
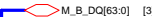


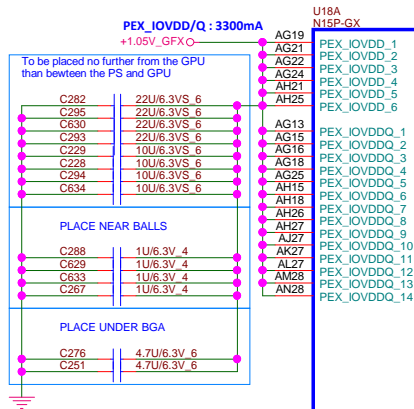
## Place these Caps near So-Dimm0.



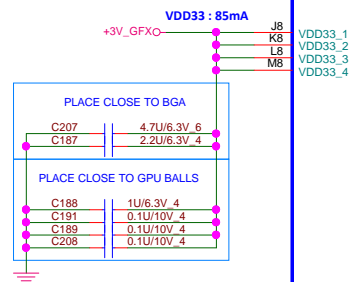
**PROJECT : TWK**  
**Quanta Computer Inc.**

Size Custom	Document Number DDR3 DIMM0-RVS (5.2H)	Rev 1A
Date: Wednesday, April 23, 2014		Sheet 12 of 42

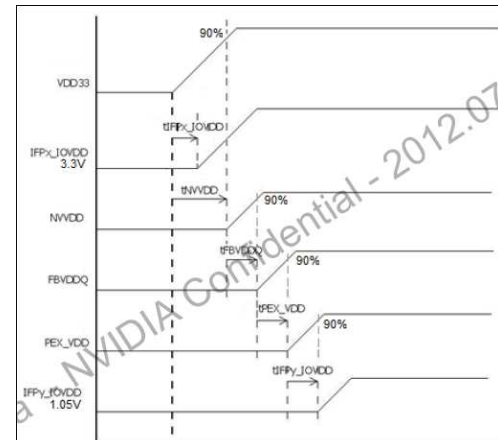
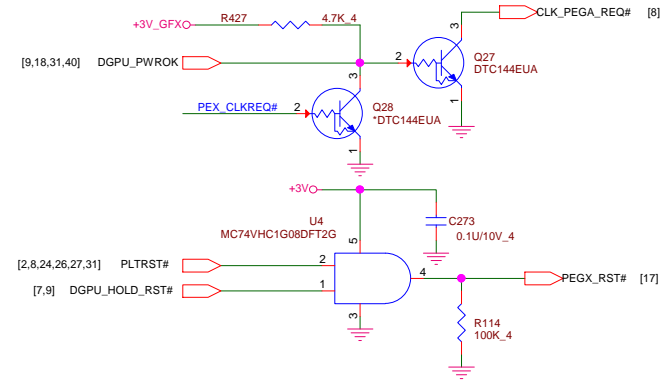
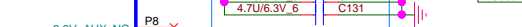
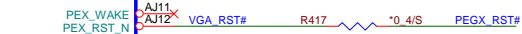
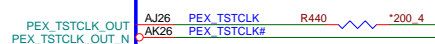
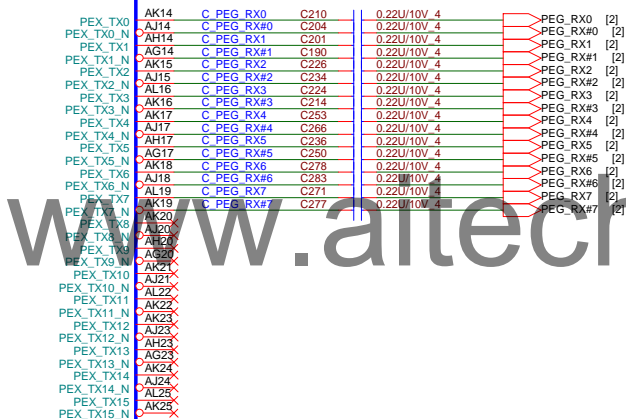
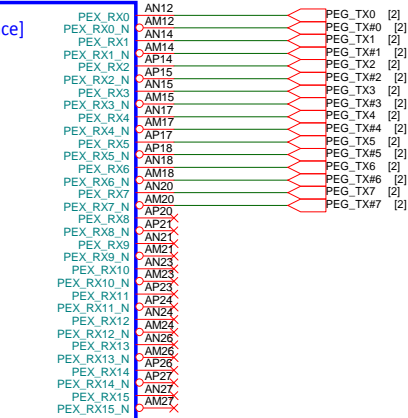




AC6 NC\_1  
AJ28 NC\_2  
AJ4 NC\_3  
AJ5 NC\_3  
AL11 NC\_4  
C15 NC\_5  
D19 NC\_6  
D20 NC\_7  
D23 NC\_8  
D26 NC\_9  
H31 NC\_10  
T8 NC\_11  
V32 NC\_12  
NC\_13



www.aitech1.ru

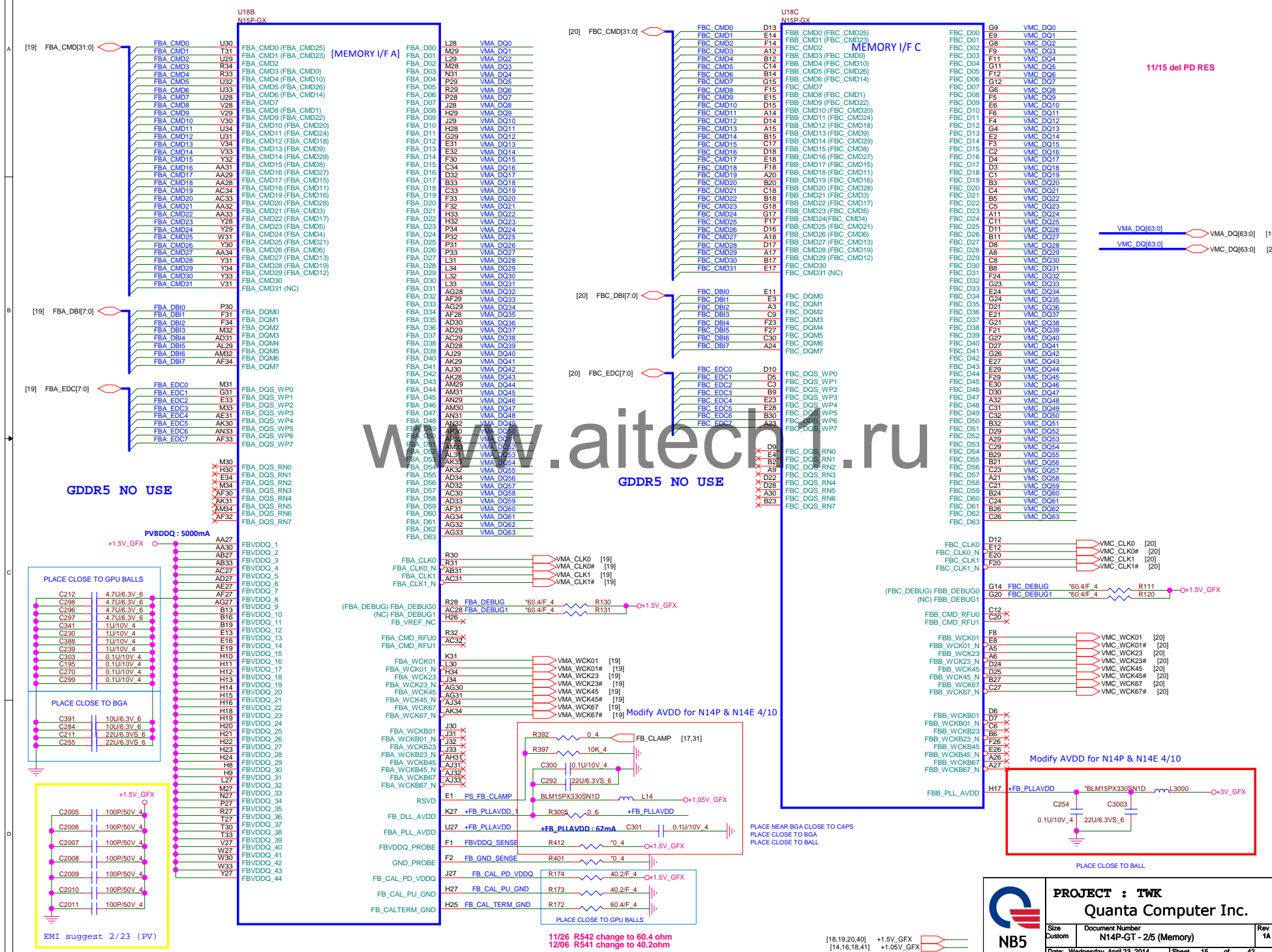


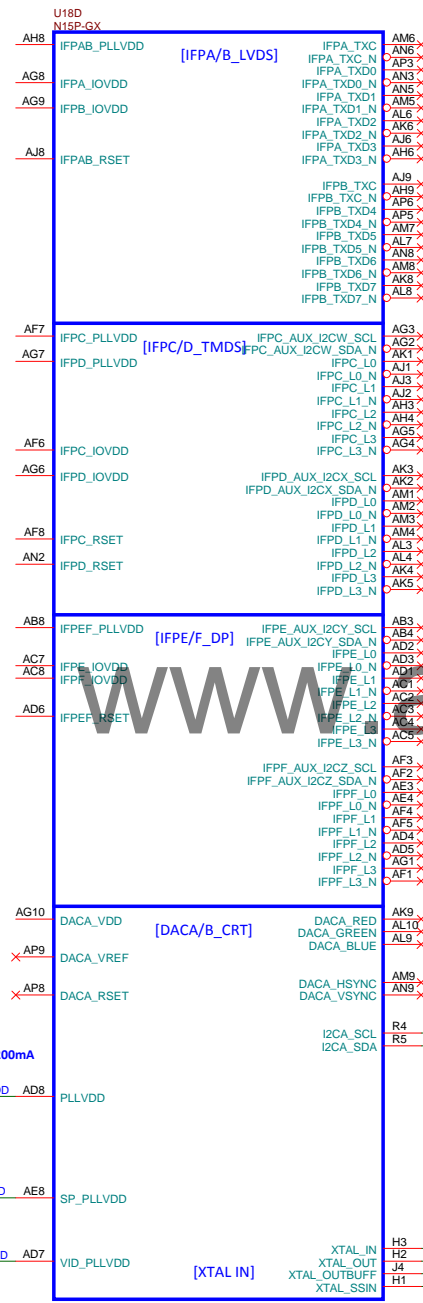
**PROJECT : TWK**  
**Quanta Computer Inc.**

Size NB5 Document Number N14P-GT - 1/5 (PCIE) Rev 1A

Date: Wednesday, April 23, 2014 Sheet 14 of 42

[15,17,18,41] +3V\_GFX  
[15,18,19,20,40] +1.5V\_GFX  
[15,16,18,41] +1.05V\_GFX  
[2,6,7,8,9,10,12,13,17,18,21,22,23,24,25,26,27,29,30,31,36,37,39] +3V

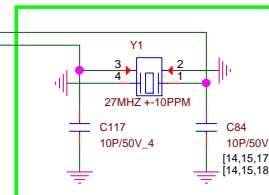





www.aitech1.ru



DV2...Change Y1 P/N and footprint  
vendor suggest change C117,C84 to 10pf 1/11



		PROJECT : TWK	
		Quanta Computer Inc.	
Size A3	Document Number N14P-GT - 3/5 (Display)	Rev 1A	
Date: Wednesday, April 23, 2014		Sheet 16 of 42	



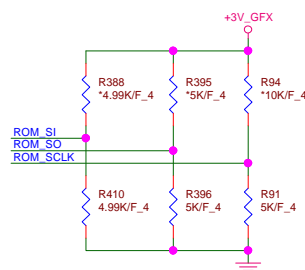
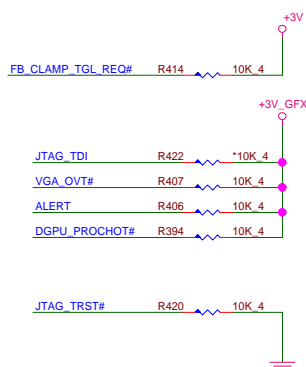
U18E  
N15P-GX

[MIOA]

[MIOB]

[MISC\_GPIO/I2C/JTAG/THER]

[MISC2\_ROM]



Default: GDDR5 Hynix 2G VRAM

Vendor	P/N	Mfr. P/N	ROM_SI	
Samsung 2G (1.35V)	AKG5MMDT502	K4G20325FD-FC03	0x00	4.99K PD
Hynix 2Gb (1.35V)	AKG5MWUTW23	H5GC2H24BFR-T2C	0x01	10KPD
Samsung 4G (1.35V)	AKG5PGDT500	K4G41325FC-HC03	0x03	20K PD
Hynix 2Gb (1.35V)	AKG5PWUTW06	H5GC4H24MFR-T2C	0x02	15K PD

N14P-GT\_Q5 device ID=0x0FB4  
N15P-GX-A2 device ID=0xi392

Netname	N14P-GT
ROM_SO	4.99K PU
ROM_SCLK	15K PD
STRAP0	45.3K PU
STRAP1	4.99K PD
STRAP2	24.9K PD
STRAP3	4.99K PD
STRAP4	45.3K PD

4.99K/F 4: CS24992FB26 RES CHIP 4.99K 1/16W +1%(0402)  
10K/F 4: CS31002FB26 RES CHIP 10K 1/16W +1%(0402)  
15K/F 4: CS31002FB24 RES CHIP 15K 1/16W +1%(0402)  
20K/F 4: CS32002FB29 RES CHIP 20K 1/16W +1%(0402)  
24.9K/F 4: CS32492FB16 RES CHIP 24.9K 1/16W +1%(0402)  
30.1K/F 4: CS33012FB18 RES CHIP 30.1K 1/16W +1%(0402)  
34.8K/F 4: CS33482FB22 RES CHIP 34.8K 1/16W +1%(0402)  
45.3K/F 4: CS34532FB18 RES CHIP 45.3K 1/16W +1%(0402)

Logical Strap Bit Mapping

Resistor Values	Pull-up to VDD33	Pull-down to GND
4.99 k	1000	0000
10.0 k	1001	0001
15.0 k	1010	0010
20.0 k	1011	0011
24.9 k	1100	0100
30.1 k	1101	0101
34.8 k	1110	0110
45.3 k	1111	0111

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	FB[1]	FB[0]	SMBL_ALT_ADDR	VGA_DEVICE
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	SOR3_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	SOR0_EXPOSED
STRAP4	RESERVED	PCIE_SPEED_CHART GE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

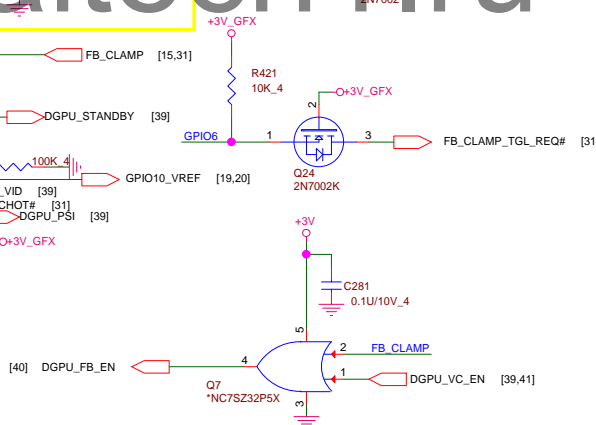
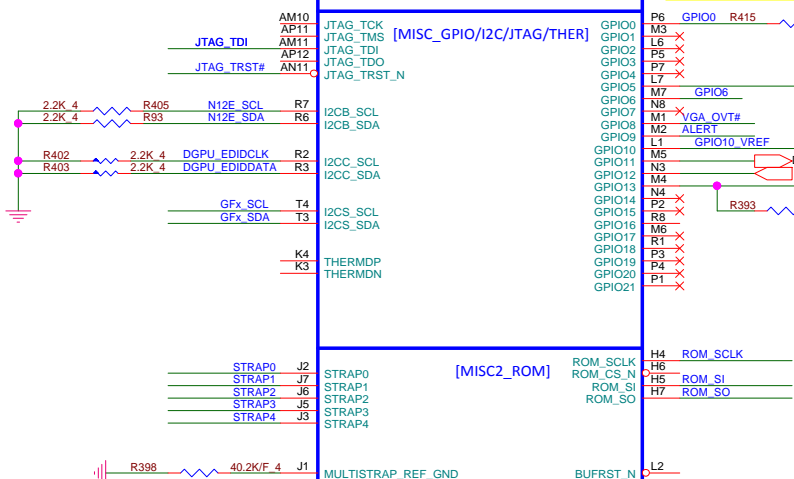
Table 9. N14P-GV/GT/GS/LP/GE GDDR5 Recommended Memories 128Mx16 Configuration

Configuration	Vendor	Strap	FBVDDQ/FBVDDQ	Manufacturer Part Number	Max Speed WCK (MHz)	Memory Date Code Minimum	Status
128Mx16 GDDR5	Hynix	0x4	1.5 V / 1.5 V	H5GQ2H244FR-T2C	2500	11/A	Production Candidate
		0x6	1.35V / 1.35V	H5GQ2H244FR-T2C	2000	11/A	Production Candidate
	Samsung	0x5	1.5 V / 1.5 V	K4G20325FD-FC04	2500	1219	Production Candidate
		0x7	1.35V / 1.35V	K4G20325FD-FC04	2000	1219	Production Candidate

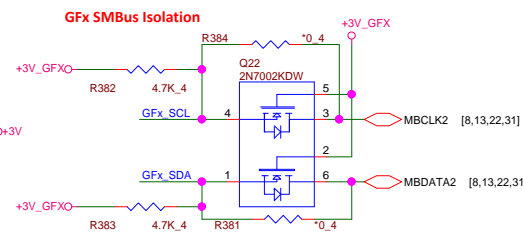
## GPIO ASSIGNMENTS

GPIO	Function
GPIO 0	Debug Service Header
GPIO 1	MEM_VDD_CTL/FAN_PWM
GPIO 2	LCD Brightness Control (BL_PWM)
GPIO 3	LCD Power Enable (PPEN)
GPIO 4	LCD Backlight Enable (BLEN)
GPIO 5	NVDD PWM_VID_BOOT_EN
GPIO 6	Remote Sensor Error Correction
GPIO 7	3D STEREO
GPIO 8	GPU Overtemp
GPIO 9	GPU Thermal Alert/FAN_PWM
GPIO 10	FB Vref Control
GPIO 11	NVDD PWM_VID
GPIO 12	PWR_Level AC Detect
GPIO 13	NVDD PSI
GPIO 14	FB_CLAMP_TGL_REG/HPD for IFP AB (not used)
GPIO 15	HPD for IFP C (DP)
GPIO 16	Fan PWM/MEM_VDD_CTL/NVDD PSI/FRAME LOCK
GPIO 17	HPD for IFP D (eDP)
GPIO 18	HPD for IFP E (DP)
GPIO 19	HPD for IFP F (DP)
GPIO 20	<not used>
GPIO 21	<not used>

www.aitech.ru

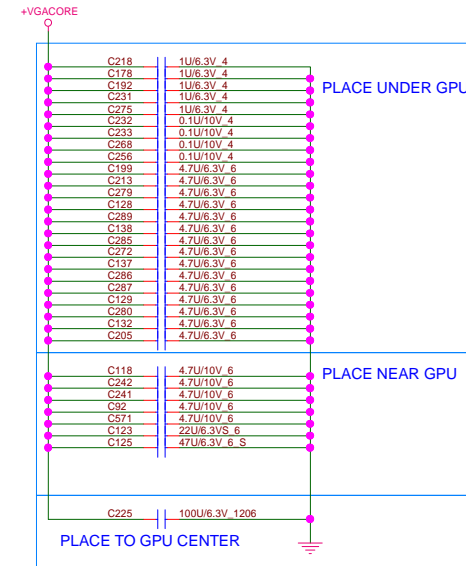
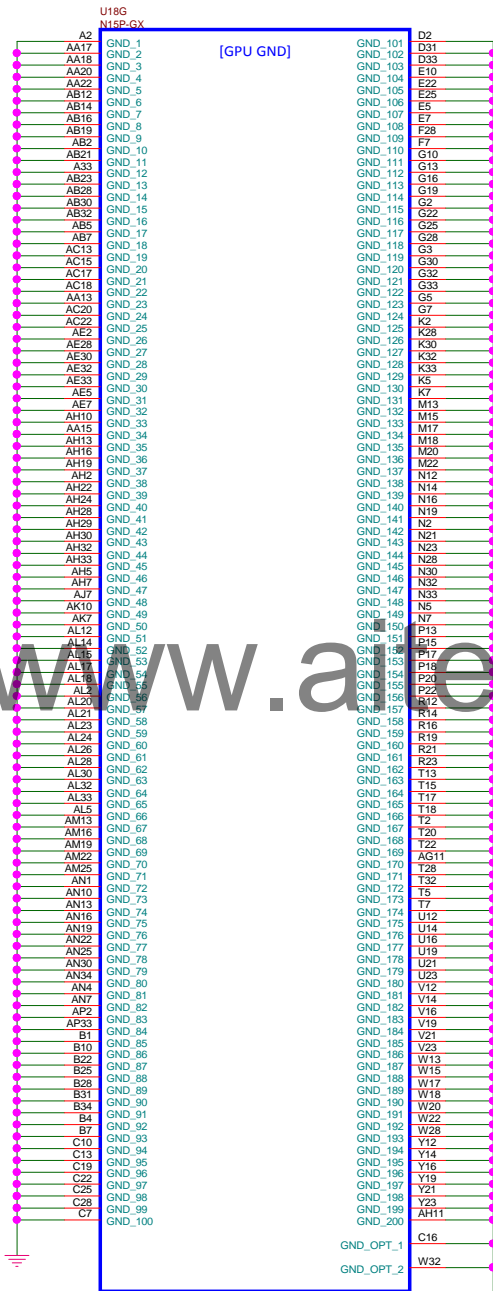
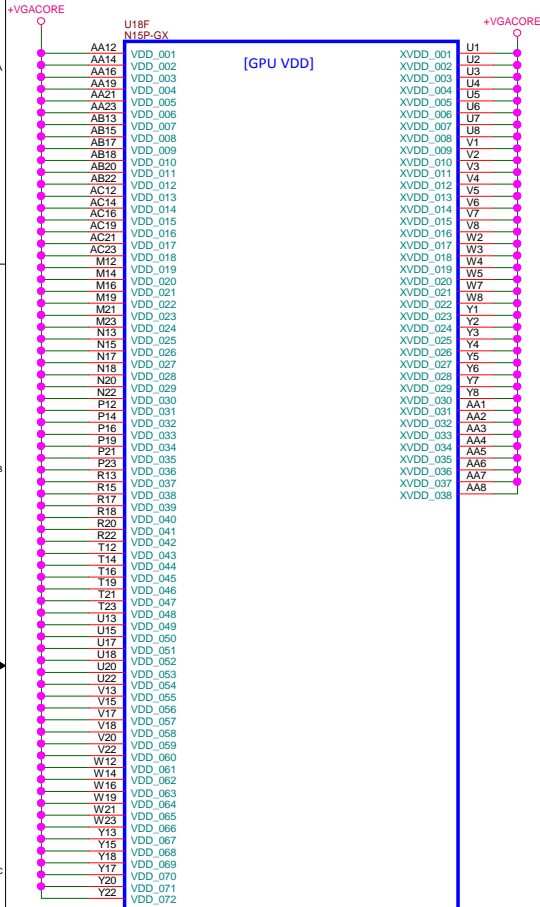


## Gfx SMBus Isolation

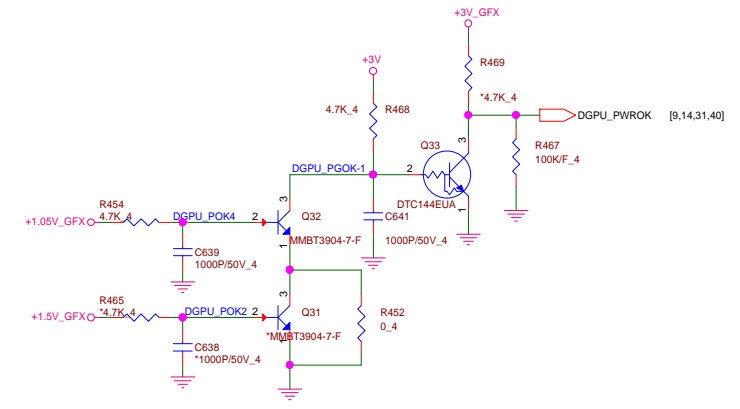
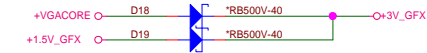
PROJECT : TWK  
Quanta Computer Inc.

Size Custom	Document Number N14P-GT - 4/5 (MISC)	Rev 1A
Date: Wednesday, April 23, 2014	Sheet 17 of 42	

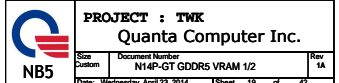
VDD/XVDD : 25.72A



for meet Power down sequence for +3V\_GFX



[39] +VGACORE  
[14,15,16,41] +1.05V\_GFX  
[15,19,20,40] +1.5V\_GFX  
[14,15,17,41] +3V\_GFX  
+3V



[15] VMC\_DQ63.0  
[15] FBC\_CMD19.0  
[15] FBC\_CMD7.0  
[15] FBC\_EDC7.0

Channel 0  
<0-31>

MF=0 Non-mirrored

QD16~23

QD0~7

Channel 0  
<32-63>

MF=1 Mirrored

QD8~15

QD24~31

Channel 1  
<0-31>

MF=0 Non-mirrored

QD48~55

QD32~39

Channel 1  
<32-63>

MF=1 Mirrored

QD40~47

QD56~63

www.aitech.ru

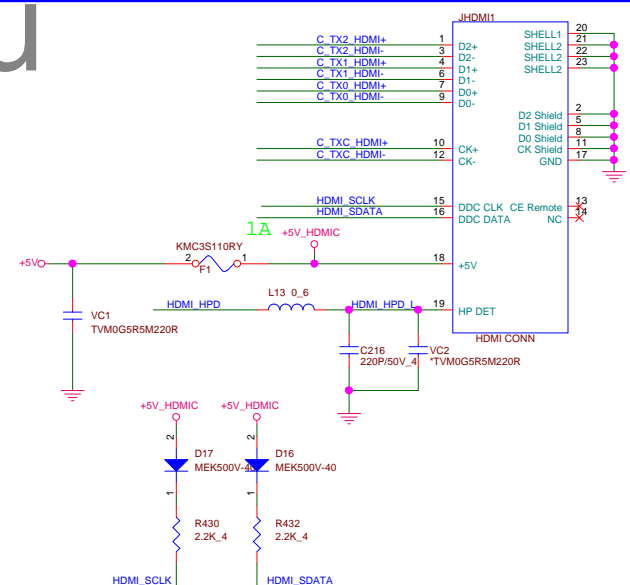
20120117 Add C764 for BMT suggestion.

CK\* is strap pin to set QDT value of memory chip

RST PD place @ the end of daisy-chain.

GDDR5 Mode H Mapping	
< 0-31 >	< 32-63 >
Cmd0	Cmd16
Cmd1	Cmd17
Cmd2	Cmd18
Cmd3	Cmd19
Cmd4	Cmd20
Cmd5	Cmd21
Cmd6	Cmd22
Cmd7	Cmd23
Cmd8	Cmd24
Cmd9	Cmd25
Cmd10	Cmd26
Cmd11	Cmd27
Cmd12	Cmd28
Cmd13	Cmd29
Cmd14	Cmd30
Cmd15	Cmd31

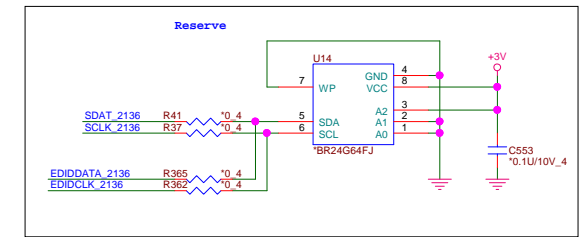
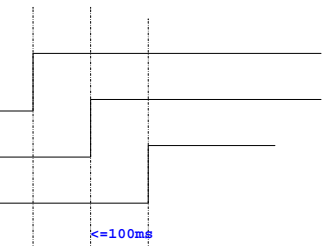
close to HDMI conn



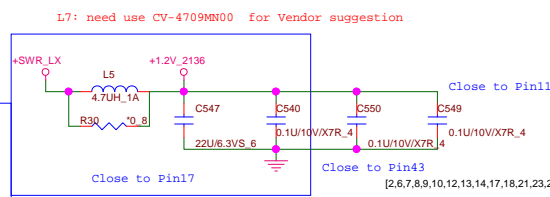
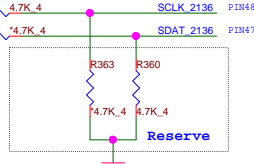
PROJECT : TWK  
Quanta Computer Inc.

Size Custom	Document Number <b>CRT,Hole</b>	Rev 1A
Date: Wednesday, April 23, 2014		Sheet 21 of 42

# RTD2136S Power Up Sequence 22



		PIN 47	
PIN 48	0	X	EP mode
	1	ROM	EEPROM



SWR MODE	LDO MODE
Stuff L69	Stuff R9095

**PROJECT : TWK**  
**Quanta Computer Inc.**

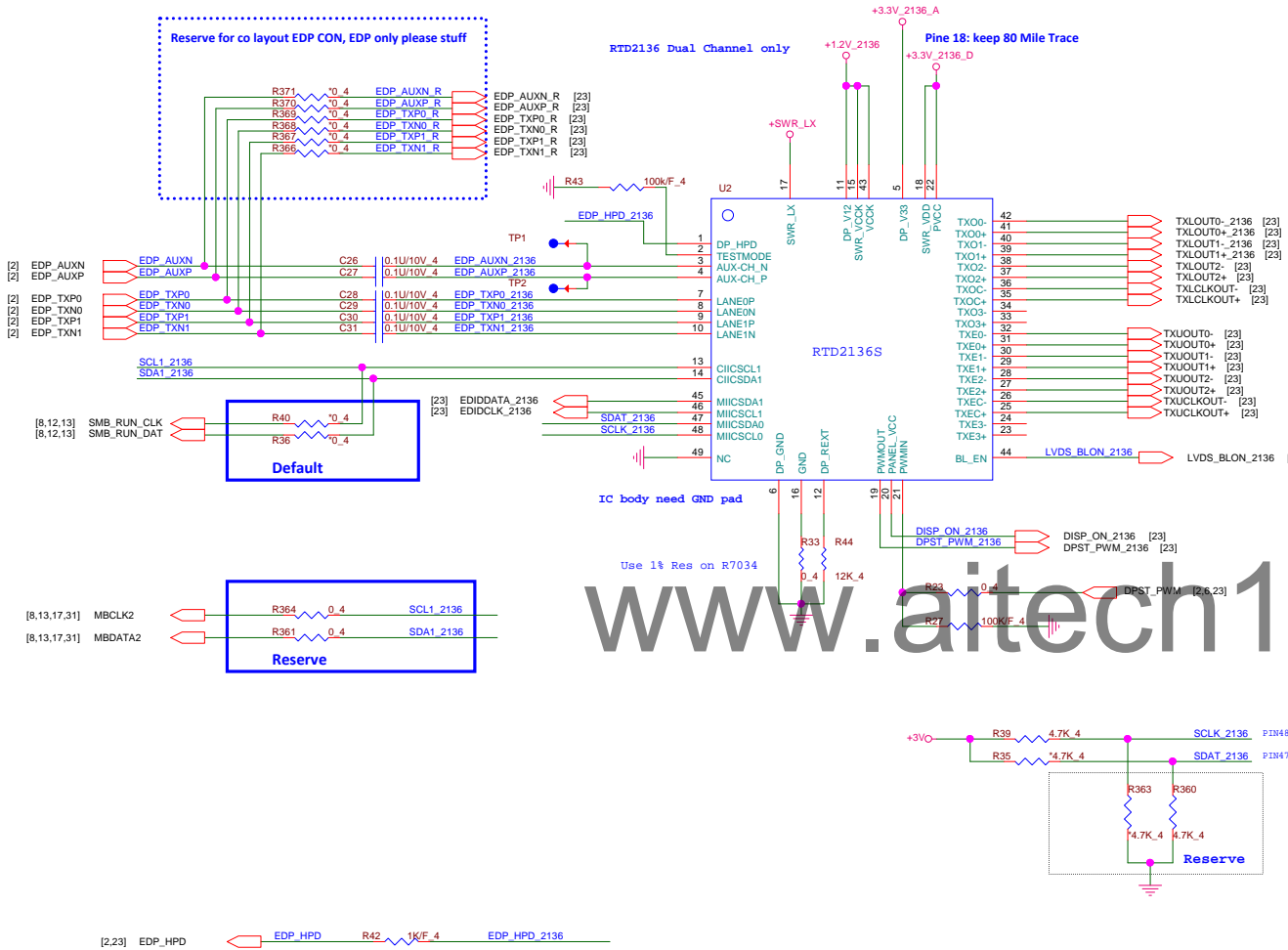
Size Custom

Document Number  
**RTD2136S**

Date: Wednesday, April 23, 2014

Rev  
1A

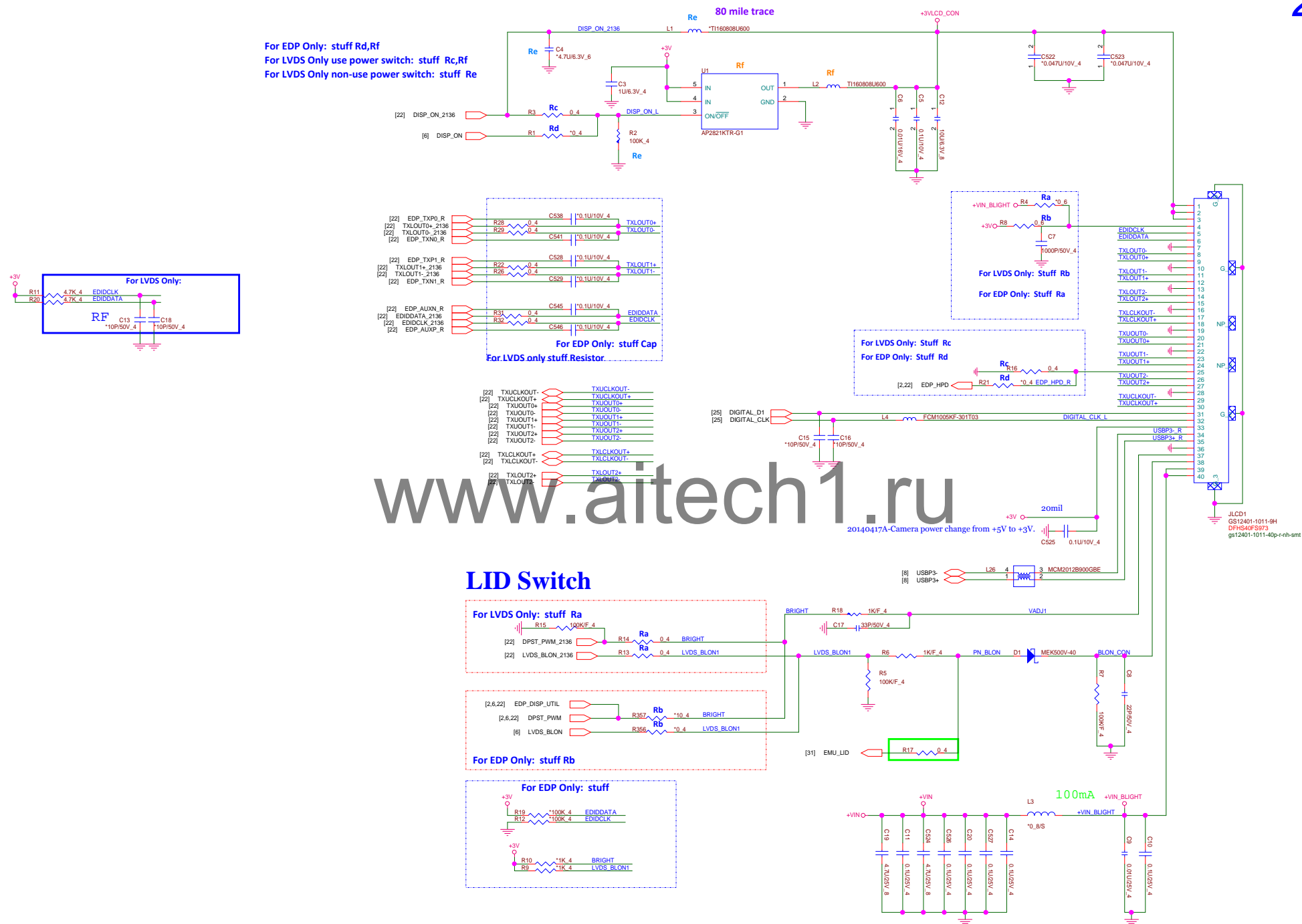
Sheet 22 of 42



www.aitech1.ru



For EDP Only: stuff Rd,Rf  
 For LVDS Only use power switch: stuff Rc,Rf  
 For LVDS Only non-use power switch: stuff Re



[2,6,7,8,9,10,12,13,14,17,18,21,22,24,25,26,27,29,30,31,36,37,39]  
 [4,7,26,28,30,31,32,33]  
 [7,21,25,26,29,30,36,39]  
 [29,32,33,34,35,37,39,40,41]

```
[8] CLK_PCIE_CRP
[8] CLK_PCIE_CRN
[8] PCIE_RXP3_CARD
[8] PCIE_RXN3_CARD
```

Please add 9 GND VIAs  
connection with thermal PAD

## R290 need colse to Chip

11/23 Add  Close to chip pin

SD / MMC  
CARD READER

CLOSE CONN

Reserve for EMI

SD D0	C720	*5.6P/16V 4
SD D1	C721	*5.6P/16V 4
SD D2	C713	*5.6P/16V 4
SD D3	C714	*5.6P/16V 4

[2,6,7,9,10,26,28,29,31,33,35,36,41] +3VS5  
[2,6,7,8,9,10,12,13,14,17,18,21,22,23,25,26,27,29,30,31,36,37,39] +3V

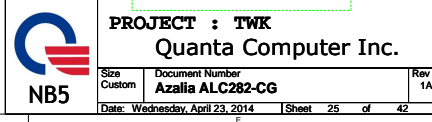


PROJECT : TWK  
Quanta Computer Inc.

Size Custom	Document Number <b>RTS5227 &amp; CR SOCKET</b>
----------------	---

Rev	1
-----	---

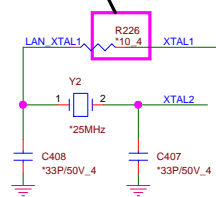
Date: Wednesday, April 23, 2014      Sheet 24 of





[2,6,7,8,9,10,12,13,14,17,18,21,22,23,24,25,27,29,30,31,36,37,39] +3V  
[7,21,25,29,30,36,39] +5V  
[4,7,28,30,31,32,33] +3VPCU  
[6,7,8,10,25,29,30,35] +1.5V

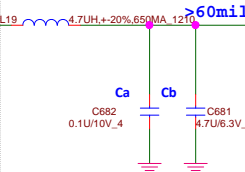
For EMI 0 ~ 22 ohm



Power trace Layout 宽度 &gt; 60mil

next ver need to add 0805 0 ohm &amp; 0.1u cap for 10/100

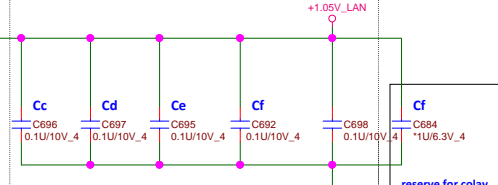
&gt;60mil

Trace < 30 mil  
Width > 60 milFor GbE  
Stuff La, Ca, CbFor 10/100  
NA: La, Ca, Cb

For GbE

\* Place Cc, Cd, Ce, Cf, Cg  
close to each VDD10 pin-- 3, 8, 22, 30

For 10/100 NA, Ce, Cf

\* Place Cc, Cd  
close to each VDD10 pin-- 8, 30 only,

For 10/100

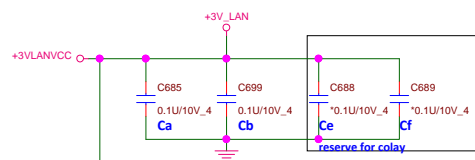
\* Place Cf close to each VDD10 pin-- 30 (reserve)

For 10/100

\* Stuff Ce and Cf only, close to each VDD33 pin-- 23, 32

For GIGA

\* Stuff Ca and Cb only, close to each VDD33 pin-- 11, 32



\* Place Cc and Cd close to each VDD33 pin-- 23, 32

For GIGA  
Stuff Cc, CdFor 10/100  
NA: Cc, Cd

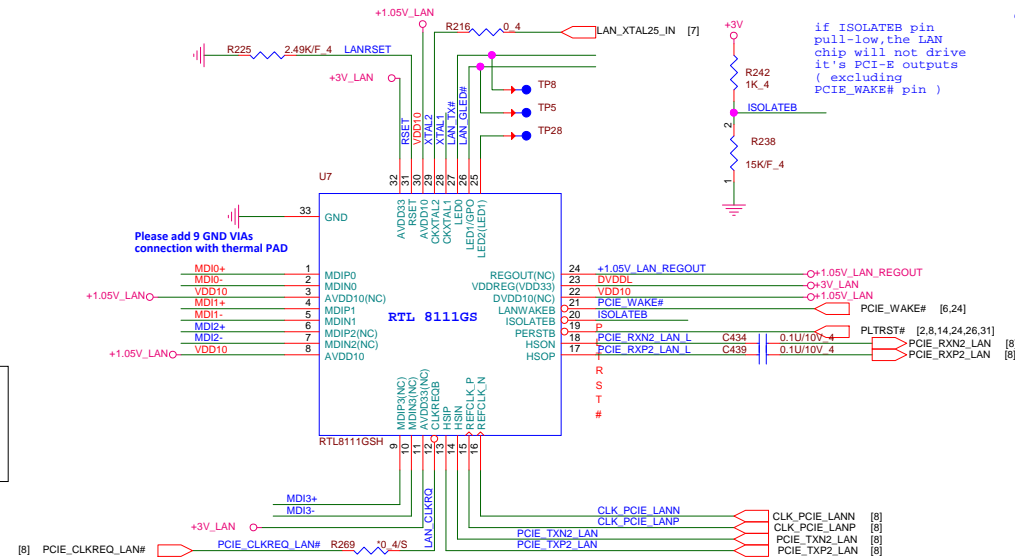
Remove For Not Using SWR mode

For GiGA

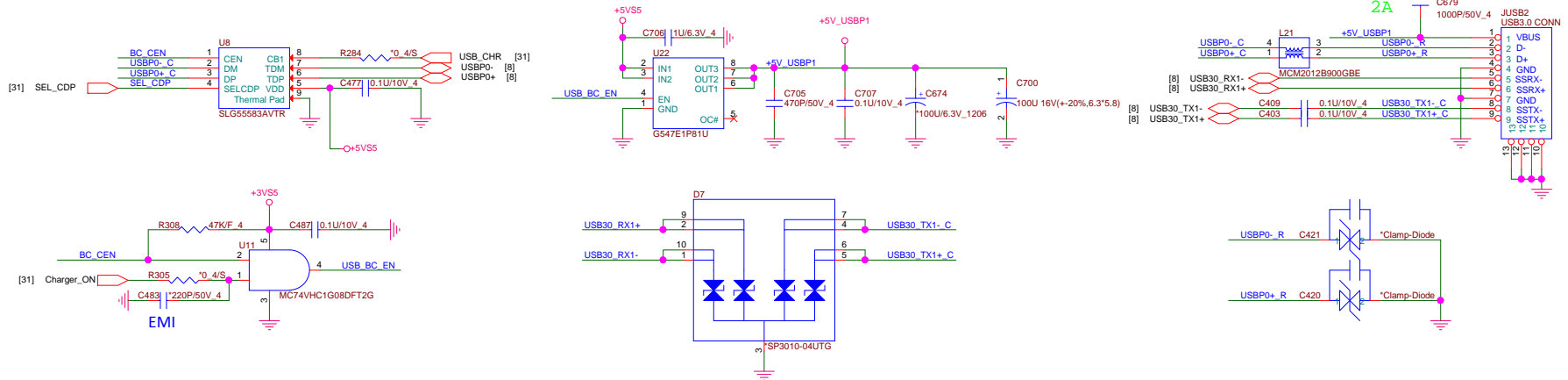
For 10/100

BOT: GST5009B LF, DB0Z06LAN00

BOT: TST1284R LF DB0EL5LAN00

[2,6,7,8,9,10,12,13,14,17,18,21,22,23,24,25,26,29,30,31,36,37,39]  
[7,36]+3V  
+3VLANVCC

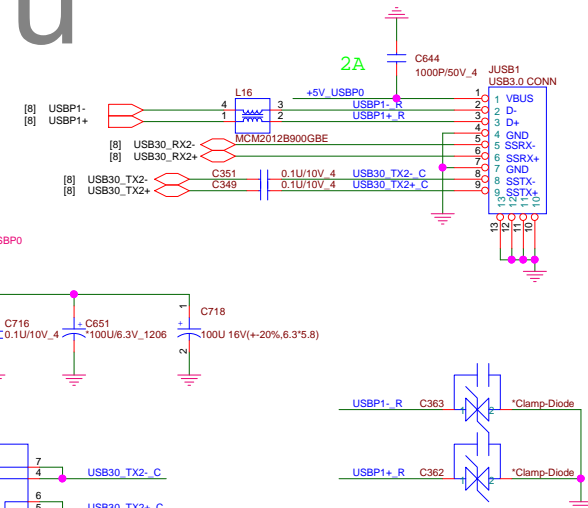
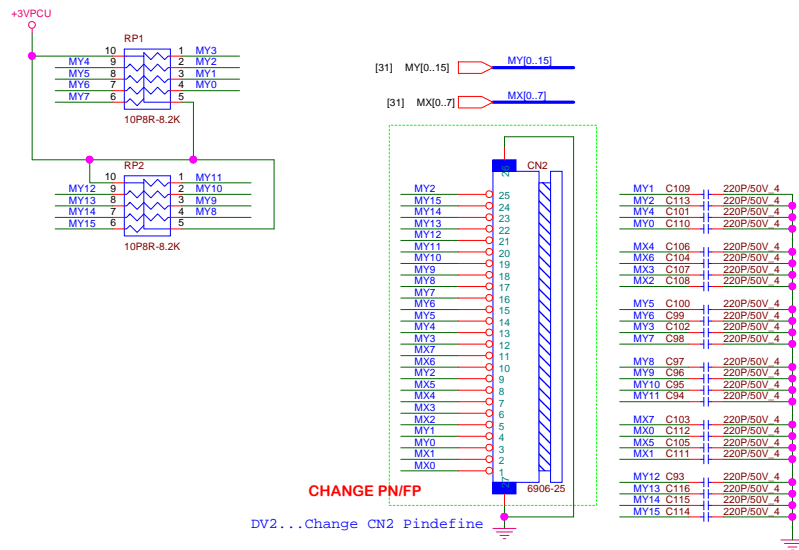
## Charge USB/USB3.0 COMBO X1



www.aitech1.ru

## USB3.0 COMBO X1

## Keyboard Connector

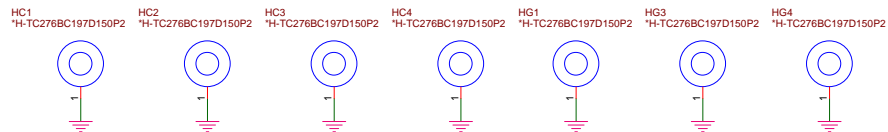


PROJECT : TWK  
Quanta Computer Inc.

Size Custom Document Number  
NB5 USB3.0/Charge USB/KBD/  
Date: Wednesday, April 23, 2014 1 Sheet 28 of 42 Rev 1A

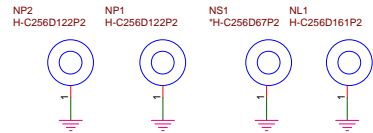


## CPU Bracket

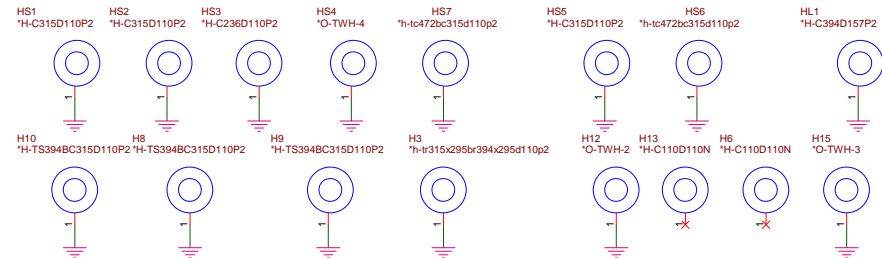


## GPU Bracket

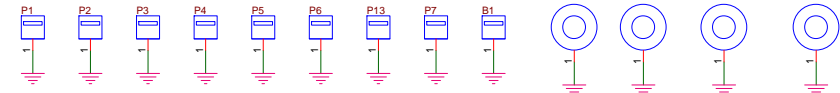
## PCH NU Screw Hold



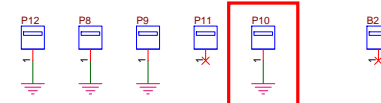
## System Screw Hold



## System Pad(Top)



## System Pad(Button)

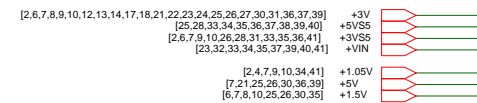
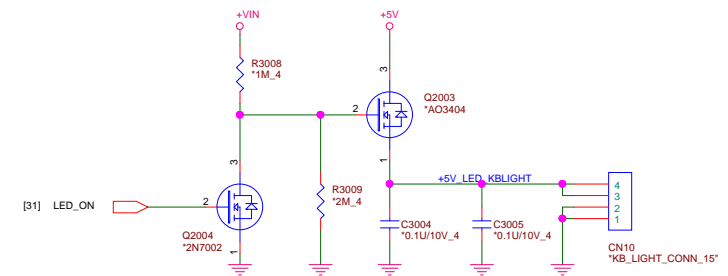
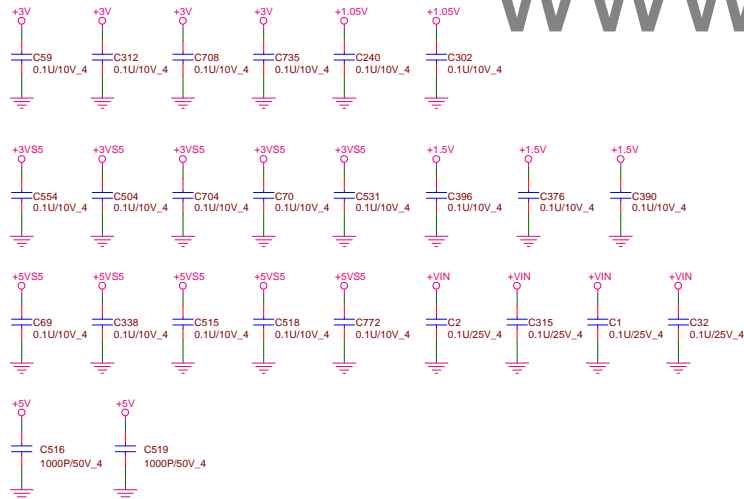


Define to GND for EMI request 4/10

www.aitech1.ru

KB LIGHT

## EMI CAP

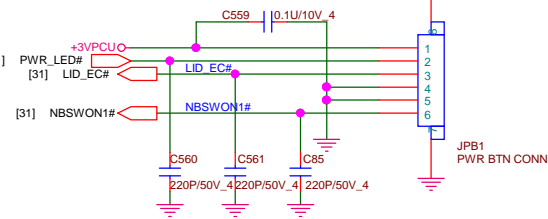


PROJECT : TWK  
Quanta Computer Inc.

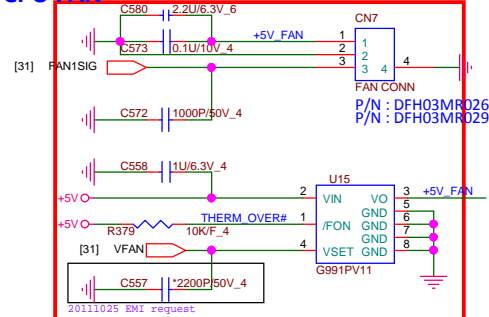
Size Custom	Document Number Hole / EMI Cap	Rev 1A
Date: Wednesday, April 23, 2014	Sheet 29 of 42	

## Power Button Connector

Pin1 : +3VPCU(LIDSWITCH PWR)  
 Pin2 : POWER LED  
 Pin3 : LIDSWITCH  
 Pin4 : GND  
 Pin5 : GND  
 Pin6 : POWERON#

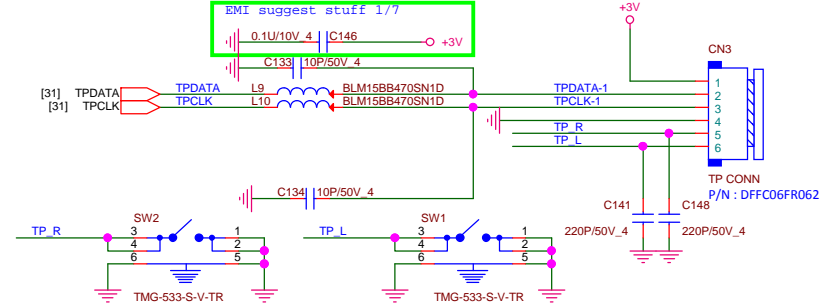


## CPU FAN

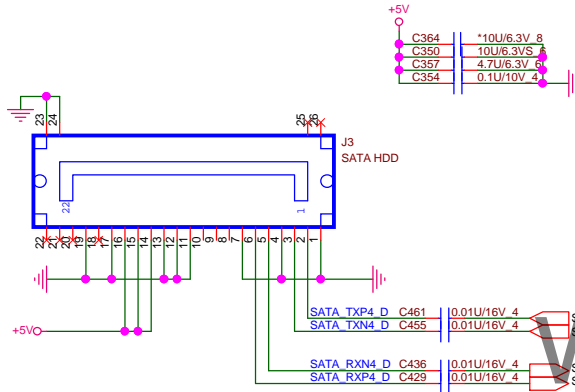


## Touch Pad Connector

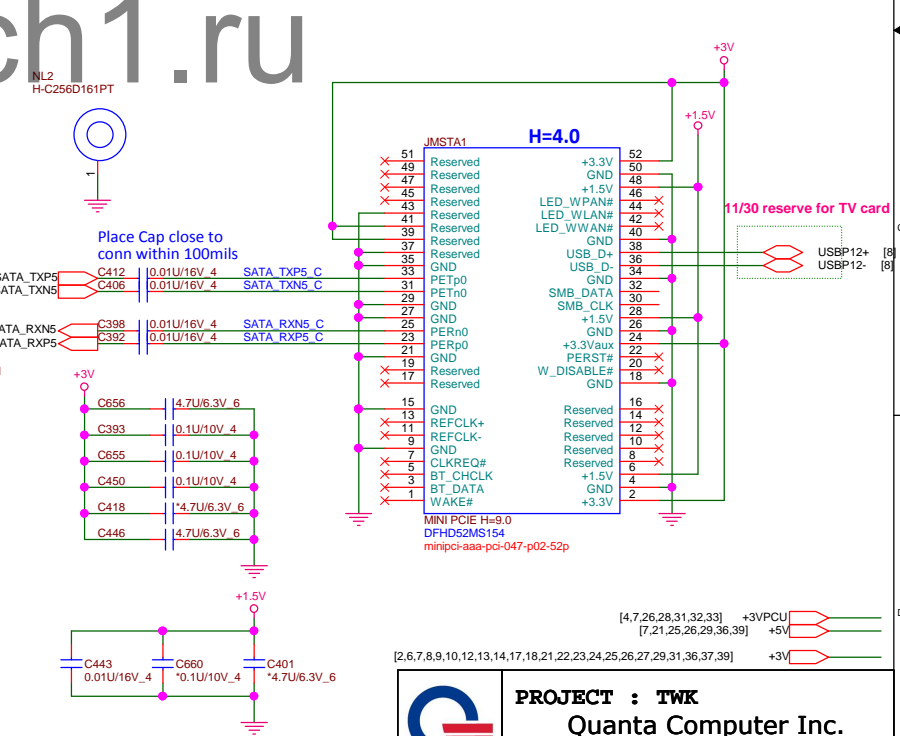
B-stage change footprint to 88513-0601-6p-l-smt



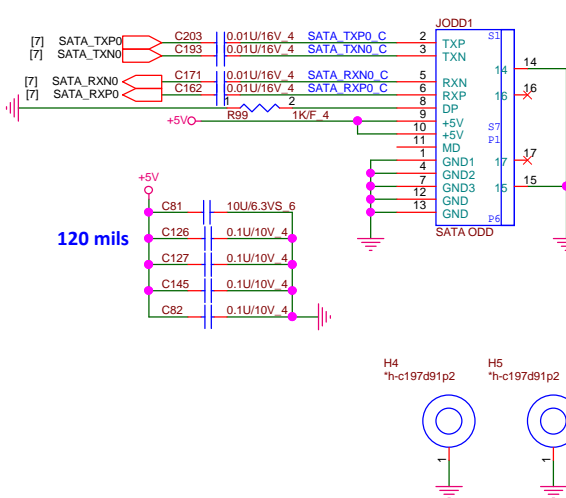
## SATA HDD CONNECTOR



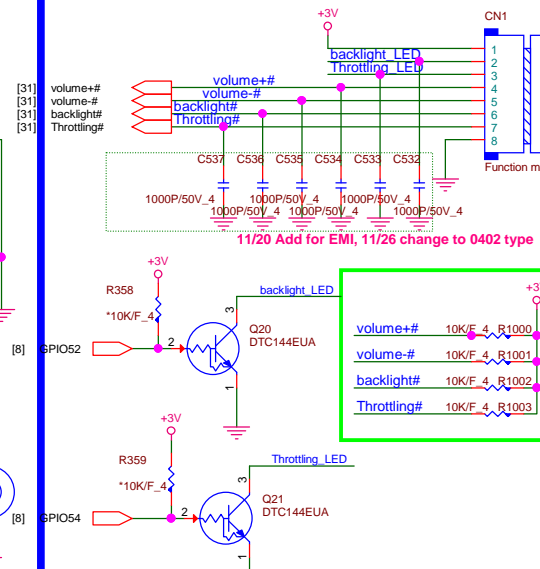
## MINISATA



## SATA ODD Connector



## Function Module connector



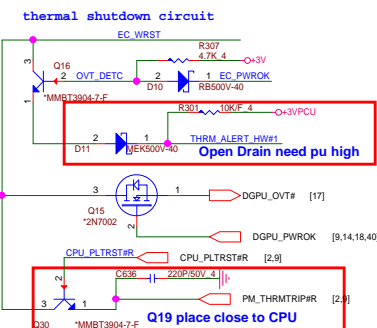
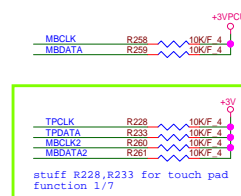
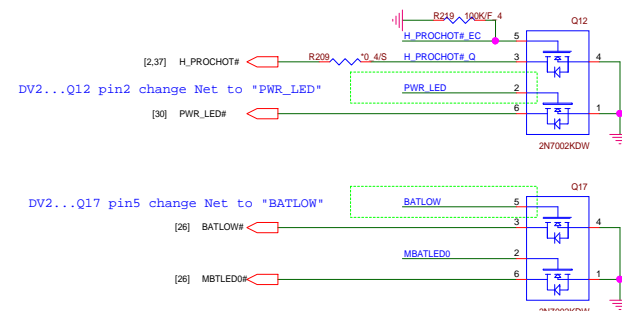
PROJECT : TWK  
 Quanta Computer Inc.



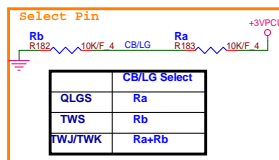
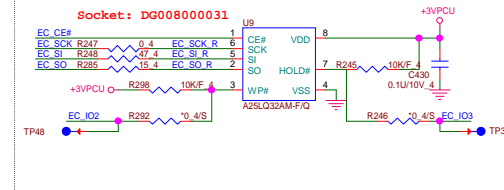
Size Custom Document Number SW/TP/FAN/HDD/ODD/mSATA Rev 1A  
 Date: Wednesday, April 23, 2014 Sheet 30 of 42



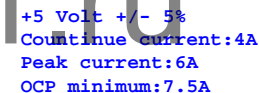
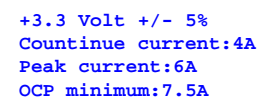
```
11/14 add
11/14 add
20140417A-Pin-30 LED_ON for TWK K/B backlight control.
```

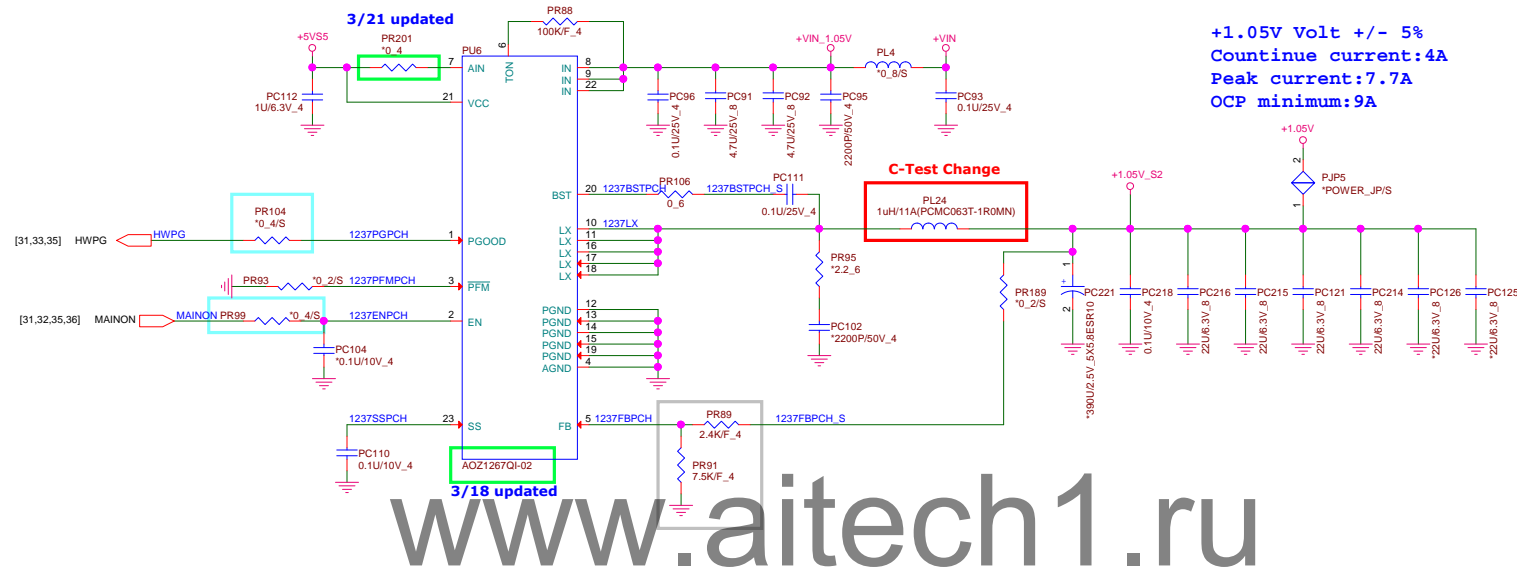


Vender	Size	P/N
AMIC	4MB	AKE39ZN0800 (AMIC A25QE32M-F (QE))
Winbond	4MB	AKE39FN0N01 (Winbond W25Q32FVSSIQ (QE))
Socket		DFHS08FS023









www.aitech1.ru

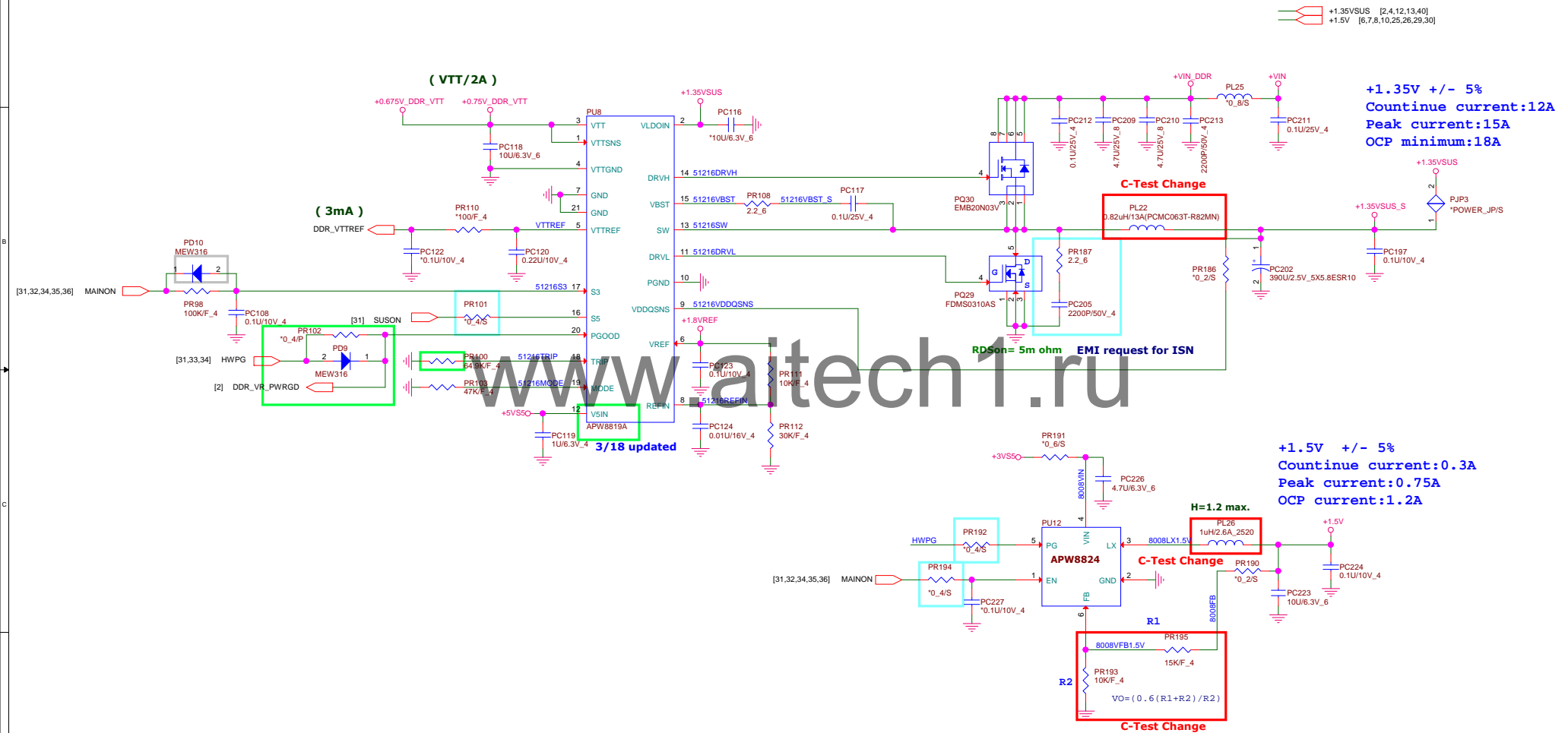
+1.05V [2,4,7,9,10,29,41]



PROJECT : TWK  
Quanta Computer Inc.

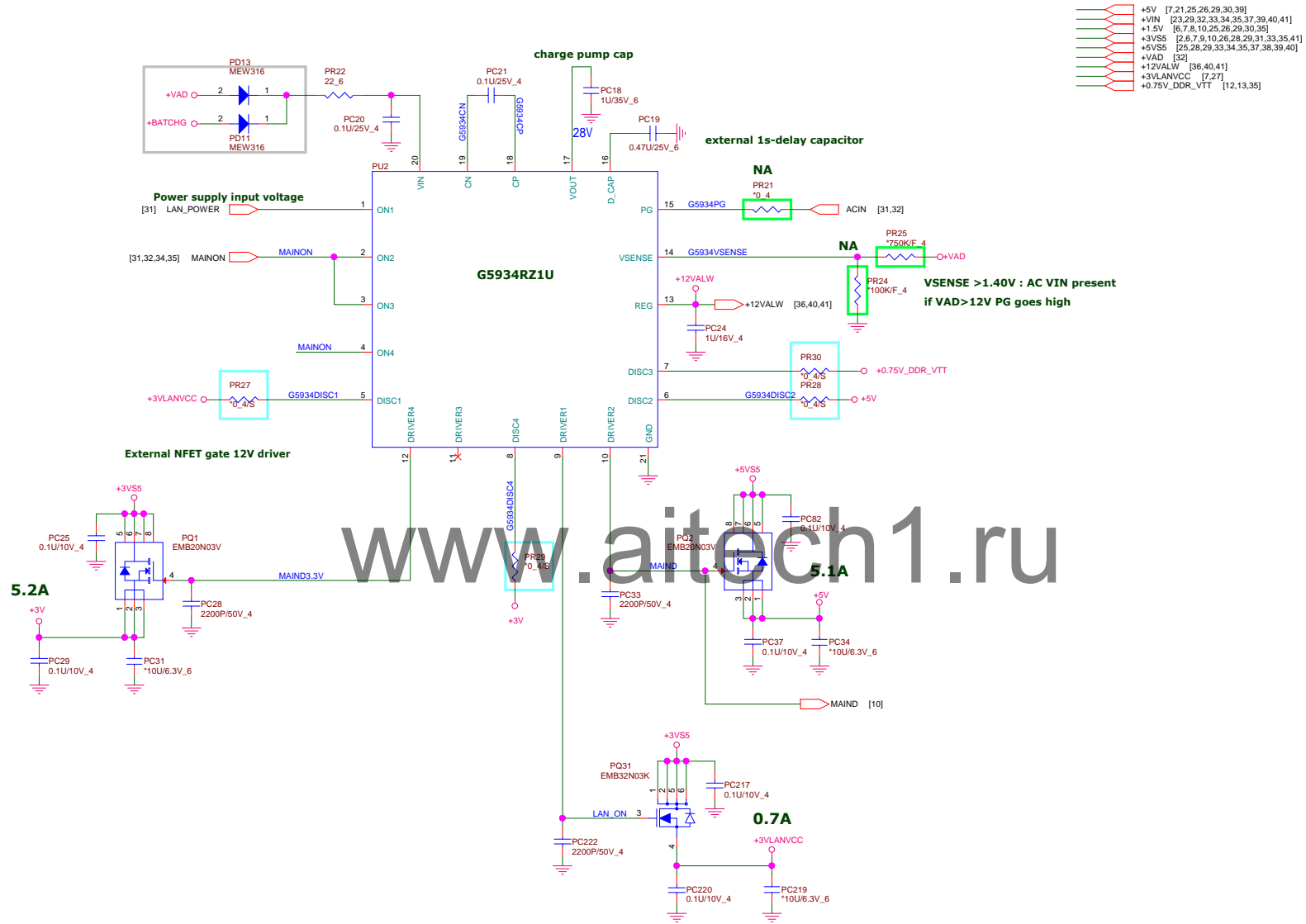
Size Custom	Document Number 1.05V(RT8228BZ)	Rev 1A
Date: Wednesday, April 23, 2014   Sheet 34 of 42		





**PROJECT : TWK**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>DDR3L(APW8819)</b>	Rev 1A
Date: Wednesday, April 23, 2014   Sheet 35 of 42		

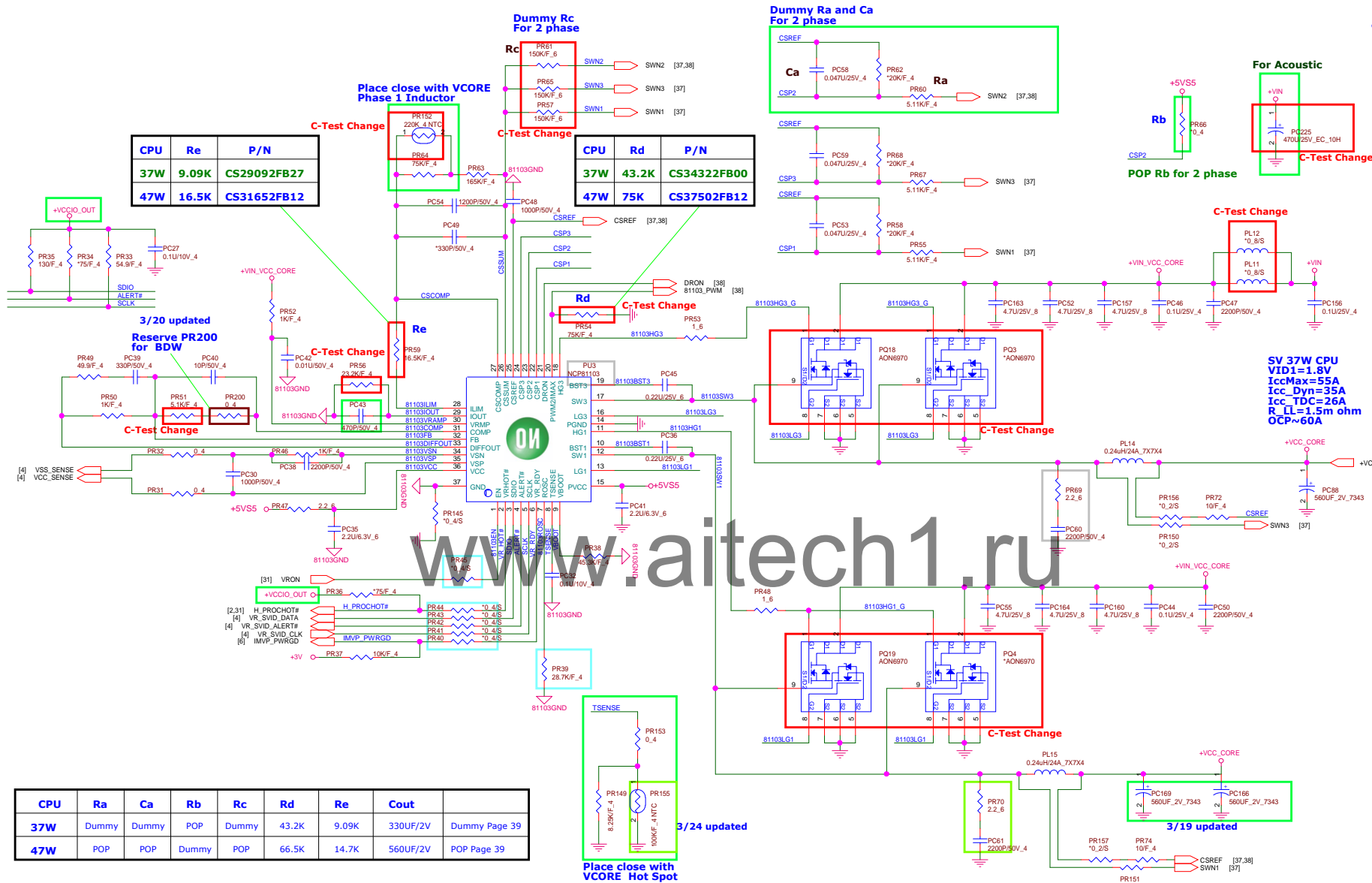


O/P will be change to shaort pad before PV

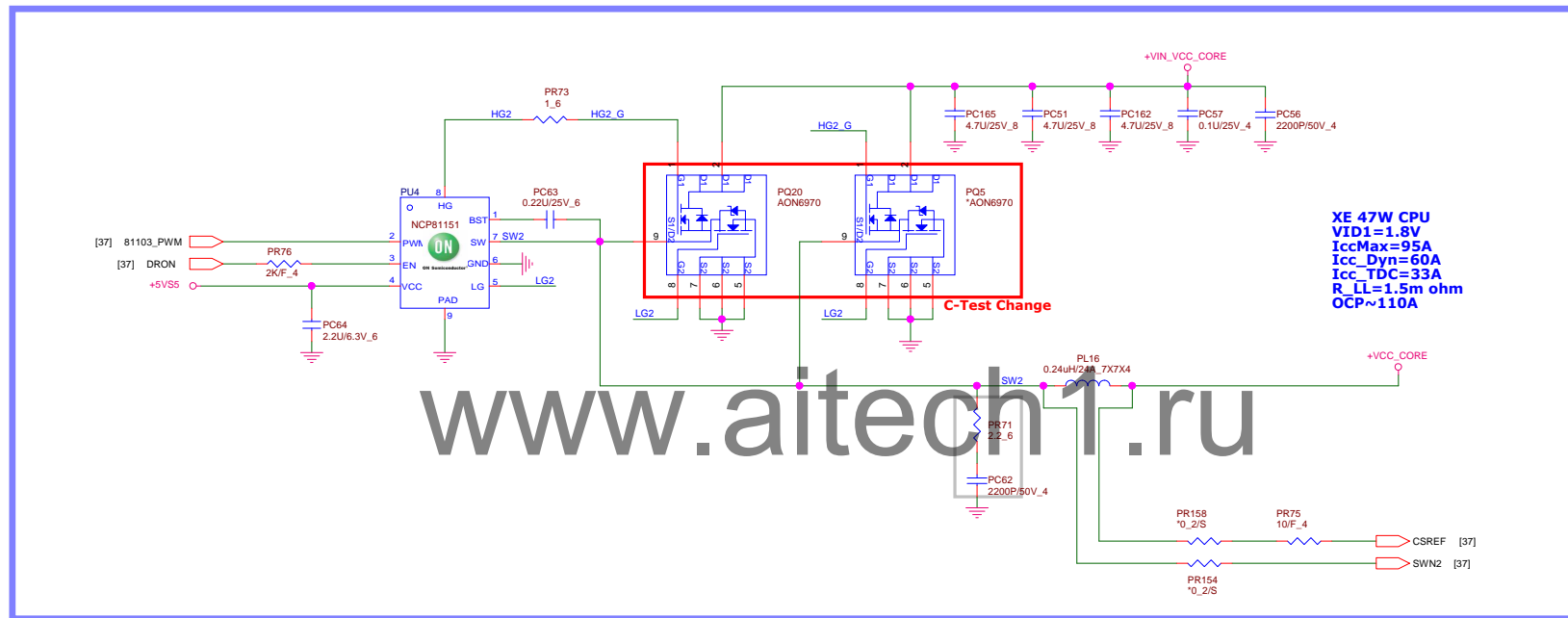


PROJECT : TWK  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Dis-charge IC (G5934)	1A
Date	Wednesday, April 23, 2014	Sheet 36 of 42



CPU	Ra	Ca	Rb	Rc	Rd	Re	Cout
37W	Dummy	Dummy	POP	Dummy	43.2K	9.09K	330UF/2V
47W	POP	POP	Dummy	POP	66.5K	14.7K	560UF/2V



+VCC\_CORE [4,37]



PROJECT : TWK  
 Quanta Computer Inc.

Size Custom	Document Number <b>NCP81151</b>	Rev 1A
Date: Wednesday, April 23, 2014		Sheet 38 of 42



